CHAPTER 10

Microwave Oscillator Design

CHAPTER OUTLINE

10.1 INTRODUCTION

An oscillator is a circuit that generates a high frequency sinusoidal waveform by converting DC energy received from a DC source. The oscillation waveform formation process in such an oscillator is shown in Fig. 10.1, which can be divided into two phases. Initially, the amplitude of the sinusoidal waveform with a specific frequency component grows exponentially in the transient state. Then, after passing through the transient state, the waveform reaches the equilibrium state where the sinusoidal waveform with constant amplitude appears.

Thus, oscillator design is to determine whether the sinusoidal waveform with the desired frequency grows exponentially for a given circuit as shown in Fig. 10.1; and then to calculate the amplitude and frequency of the oscillation waveform at equilibrium. Thus, for a given circuit, the condition necessary for a sinusoidal waveform with specific frequency to grow exponentially is called an oscillation start-up condition or simply oscillation condition. The oscillation condition which tells whether the sinusoidal waveform with a specific frequency can grow exponentially or not for a given circuit can be analyzed based on small-signal as the signal level in oscillation start-up is low. In contrast, since the signal level is not low enough at equilibrium, large signal analysis must be carried out. Therefore, the oscillation condition at equilibrium or simply equilibrium condition should be described using large-signal parameters. Since active devices such as transistors are generally nonlinear, it is not possible to directly apply the linear circuit analysis concept such as impedance or reflection coefficient to describe the oscillation condition at equilibrium. However, since the level of harmonics in an oscillator circuits is low, large-signal impedance or gain can be

defined by extending the concept of small-signal impedance or gain to describe the oscillation condition at equilibrium.

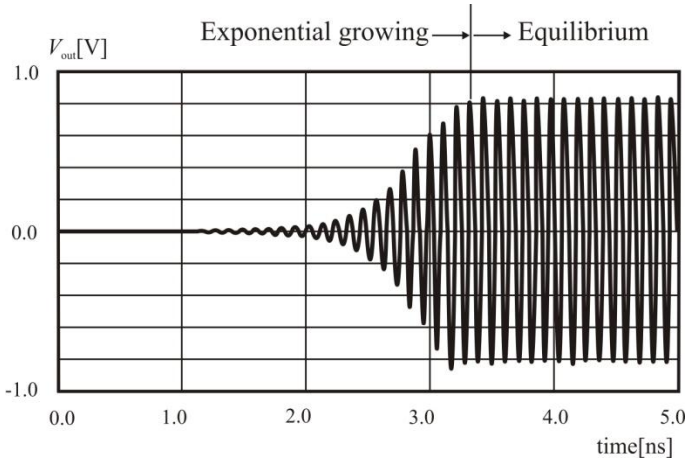

Figure 10.1 Formation of oscillation waveform

In this chapter, not only the oscillation start-up but also equilibrium conditions will be described. The large-signal impedance and reflection coefficient will be used to describe the equilibrium oscillation condition. Next, we will learn about the transformation of oscillator circuits and their design. In addition, the oscillation waveform is not an ideal sinusoidal waveform and the amplitude and phase of the sinusoidal waveform varies randomly with time, the model and measurement technique of which will be discussed in this chapter.

10.2 OSCILLATION CONDITIONS

The small-signal oscillation (*start-up condition*) and large-signal equilibrium oscillation conditions of an oscillator circuit are described in a number of ways. The reason for the various descriptions for the oscillation conditions is related to the ease of measurement and depends on the availability of active devices according to historical development. However, although the descriptions of the oscillation conditions may differ, they describe the same oscillation phenomena.

Earlier microwave oscillators were implemented using mainly 1-port devices such as Gunn or IMPATT diodes, which is why it was necessary to describe the oscillator based on one-port oscillations condition. The one-port network can easily be described using the impedance or reflection coefficient and can be measured directly. Thus, it is convenient to describe oscillation condition and equilibrium oscillations condition by the impedance or reflection coefficient defined for a given oscillator circuit. As network analyzers are generally used in microwave circuit measurements, the reflection coefficient is more direct and preferred than impedance. Thus oscillation condition based on reflection coefficient from the two oscillation conditions is commonly used. Also the oscillation conditions in ADS are based on the reflection coefficient. However, the impedance-based oscillation conditions can still be applied to an oscillator circuit after converting reflection coefficient into impedance.

Due to recent advances in microwave semiconductor technology however, pHEMT, HBT, and transistors are mainly used in microwave applications instead of one-port devices such as Gunn

diode or IMPATT diode. Thus, instead of the oscillation condition based on one-port parameters such as impedance and reflection coefficient, a technique based on open-loop gain is more convenient. In other words, since the oscillation of these two-port devices such as transistors are in general implemented by feedback network, the open-loop gain oscillation condition is obviously easy to apply. In this chapter, we would explain the oscillation conditions for these oscillator circuits using two-port devices.

10.2.1 Oscillation Conditions Based on Impedance

10.2.1.1 Start-up Condition

The oscillator, using the one-port circuit, can be viewed as a circuit composed of a 1-port load connected to a 1-port active part as shown in Fig. 10.2. In this circuit, the active part represents the one-port circuit which includes an active device such as the Gunn diode or IMPATT diode, and has a negative resistance. The impedance of the active device in general, depends on the amplitude of the RF current I as shown in Fig 10.2. Thus, $Z_A(I,\omega)$ represents the large signal impedance. The detailed computations (using ADS or measurements of large signal impedance, reflection coefficient, and gain) of which can be found in Appendix D. On the other hand, the load circuit can be considered as a passive circuit which includes the load, and depends on frequency alone. These individual impedances of the active and load part can easily be measured using network analyzer. Defining the impedance as shown in Fig. 10.2, the sum of the two impedances can be expressed as

$$\begin{aligned} R + jX &= Z_A(I,\omega) + Z_L(\omega) \\ &= R_A(I,\omega) + R_L(\omega) + j\left(X_A(I,\omega) + X_L(\omega)\right) \end{aligned} \tag{10.1}$$

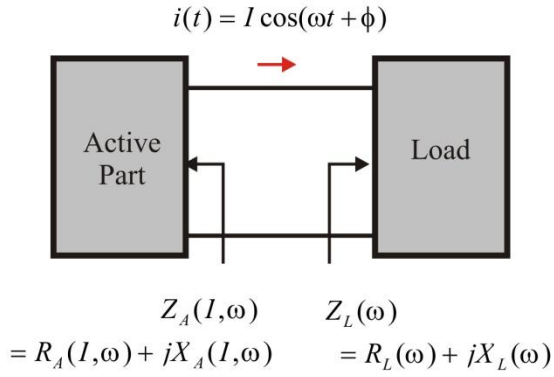

Figure 10.2 Oscillator circuit with 1-port load connected to the active part

Near the oscillation start-up point, the signal is considered as small signal, and since $I \cong 0$, equation (10.1) can be written as

$$R(0,\omega) + jX(0,\omega) = R_A(0,\omega) + R_L(\omega) + j\left\{X_A(0,\omega) + X_L(\omega)\right\} \tag{10.2}$$

Let the frequency at which the imaginary part $X(0, \omega) = 0$ be ω_o. At such ω_o, when $R(0, \omega) < 0$, the current I grows exponentially with frequency ω_o, which can be seen to satisfy the oscillation start-

up condition. That is, in order to start the oscillation, the following conditions must be satisfied, and their frequency-dependent variations are as shown in Fig. 10.3.

$$R(0,\omega)<0, \quad X(0,\omega)=0 \tag{10.3a}$$

$$\left.\frac{\partial X}{\partial \omega}\right|_{\omega=\omega_o} > 0 \tag{10.3b}$$

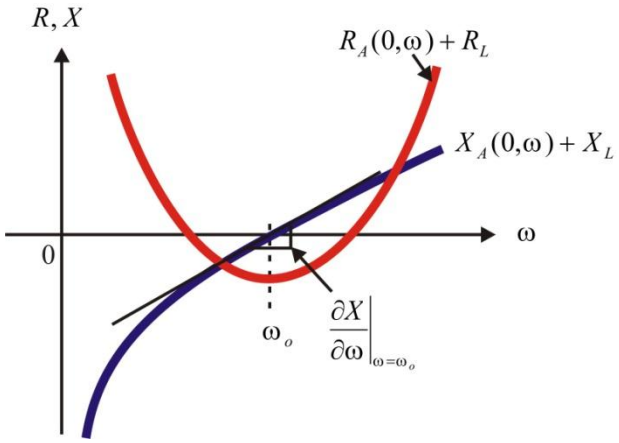

Figure 10.3 Series oscillation condition

It must be noted that equation (10.3b) can be interpreted as a series resonant condition, and oscillation does not occur when the condition in (10.3b) is not satisfied. This is the description of the oscillation condition in terms of impedance; a similar description can be obtained in terms of admittance. The load and active part in Fig. 10.2 can be viewed of as connected in series, however, the same connection can also be considered as a parallel connection as shown in Fig. 10.4. When viewed as a parallel connection, voltage is common to the two 1-port circuits, whereas in the case of a series connection, current is common.

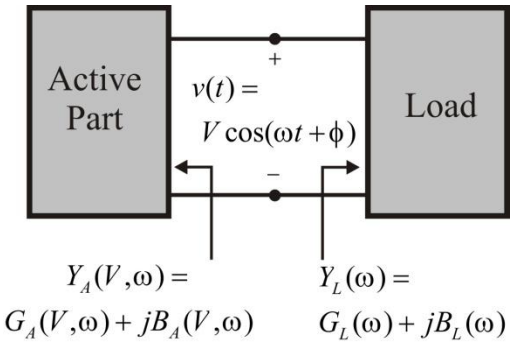

Figure 10.4 Oscillator circuit with 1-port load connected to the active part

The admittances of the active part and load circuit respectively, are defined as follows:

$$Y_A(V,\omega) = G_A(V,\omega) + jB_A(V,\omega)$$

$$Y_L(\omega) = G_L(\omega) + jB_L(\omega)$$

Denoting the sum of the admittances as $Y = G + jB$, then similarly,

$$G(0,\omega) < 0, \quad B(0,\omega) = 0 \tag{10.4a}$$

$$\left.\frac{\partial B(0,\omega)}{\partial \omega}\right|_{\omega=\omega_o} > 0 \tag{10.4b}$$

are the start-up conditions that must be satisfied for the oscillation waveform to grow exponentially. Also noteworthy is that, in the impedance oscillation condition, the amplitude of RF current increases exponentially, whereas in the admittance oscillation condition, it can be seen that it is the amplitude of RF voltage that increases exponentially.

It should be noted that when the impedance and admittance oscillation conditions discussed in equation (10.3) and (10.4) are applied to a fixed load, the impedance oscillation condition appears not to be satisfied when viewed from the admittance oscillation conditions and vice versa. To investigate this, we considered the case when a fixed load (for example, Z_o = 50 ohm load) is connected to the series resonating active part as shown in Fig. 10.5(a). Assuming the sum of the active part and load impedances satisfies the oscillation condition given by equation (10.3) near the frequency ω_o, then, $-r + Z_o < 0$ and at the same time $X(\omega_o) = 0$ and the slope is positive.

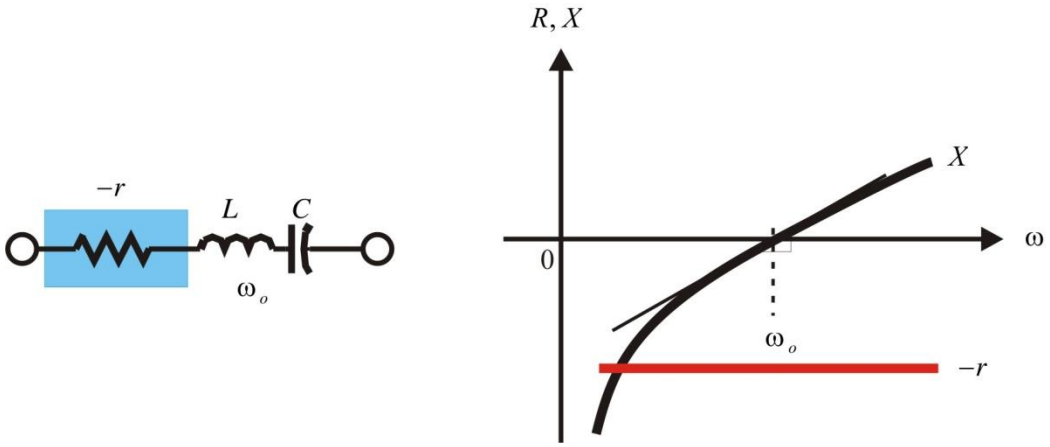

Figure 10.5 (a) Equivalent circuit of the active part (b) frequency-dependent impedance of the active part

However, considering the active part impedance as an admittance,

$$Y = \frac{1}{Z} = \frac{-r}{r^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} + \frac{-j\left(\omega L - \frac{1}{\omega C}\right)}{r^2 + \left(\omega L - \frac{1}{\omega C}\right)^2},$$

the admittance can be represented as in Fig. 10.6.

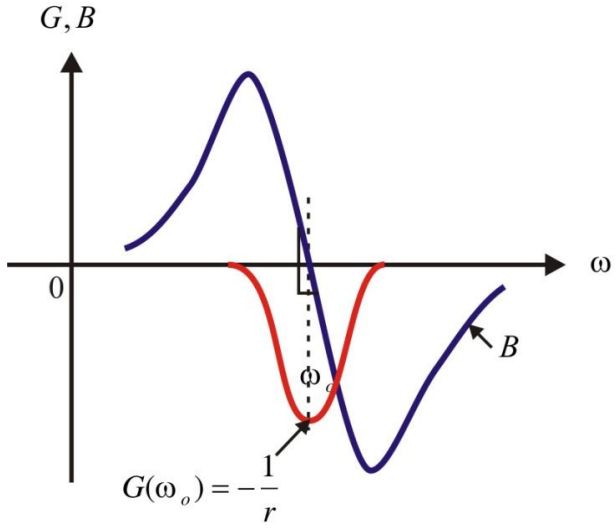

Figure 10.6 The admittance corresponding to the impedance of Figure 10.4

The sum of the load conductance and the real part of Y at ω_o becomes

$$-\frac{1}{r} + Y_o = \frac{-Z_o + r}{rZ_o} > 0$$

That is, as the total conductance is positive, this does not satisfy an admittance oscillation condition for which the amplitude of voltage will grow exponentially. Thus, for the impedance condition in (10.3), which satisfies the oscillation condition, the oscillation condition is not satisfied when viewed as admittance. Similarly, when the admittance oscillation condition is viewed as impedance, the oscillation condition is not satisfied.

Notably, the slope of the susceptance B can be seen to be negative. Thus, even when it shows positive conductance, if the slope of B at B=0 is negative; it must be re-investigated whether the impedance oscillation condition is satisfied or not. Similarly, in terms of impedance, even though the total resistance R is positive, a point where the reactance X is 0 occurs, and if the slope of X is negative, it must be re-investigated whether the admittance oscillation condition is satisfied or not.

The reason for this is that, the impedance oscillation condition describes the condition for current amplitude to grow exponentially, which is not the exponential growth in terms of the voltage amplitide. This is so because, the current growth condition viewed from the voltage view point is an entirely different growth condition.

■ Example 10.1

The active part of a series resonant oscillator connected to a load through a 1/4 wavelength impedance inverter is shown in Fig. 10E.1. To convert the load impedance of 50 ohms into 10 ohm, the characteristic impedance of the inverter was set to $Z_o=(10\times50)^{\frac{1}{2}}=22.4$. Discuss the oscillation condition at the plane of the load side and the oscillation condition at the plane of the active part.

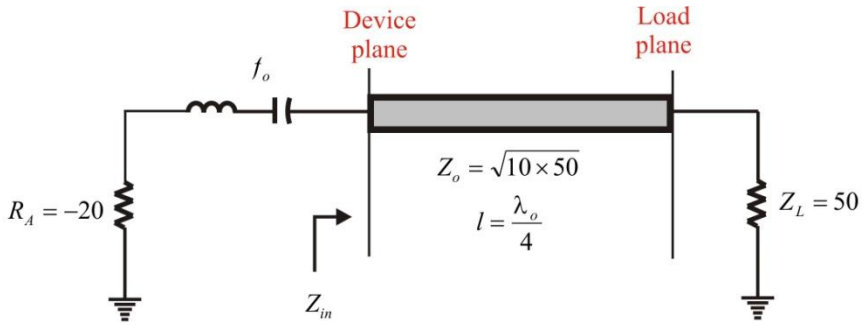

Figure 10E.1 Example of oscillation circuit

Solution

When the load impedance is seen from the active part, the impedance of 10 ohm appears at the active part through the impedance inverter. A series resonant circuit is formed at device plane and series oscillation will occur. Thus RF current amplitude with the resonance frequency will grows. Conversely, when the active part is transformed to the load side through the impedance inverter, the real part becomes $Z_a=-(Z_o)^2/20=-25$ ohm, which is smaller than the real part of the load. However, the output impedance at the load side is given by,

$$Z_{out}=\frac{Z_o^2}{R_A+jX_A} \tag{10E.1}$$

The above equation means that the series connection is transformed to a parallel connection through the impedance inverter and a parallel resonant circuit appears at the load side. Thus, because the real part of the active part is smaller than the load, it can be seen to satisfy the parallel oscillation condition. Therefore, at the load side, a growth condition of RF voltage is satisfied. In conclusion, by changing the reference plane, the series-formed oscillation condition can be changed into parallel oscillation condition.

■

■ Example 10.2

The computed result of the sum of the series impedance $R(0,\omega)+jX(0,\omega)$ between the active part and the load, were obtained as shown in Fig. 10E.2. Explain where oscillations can occur; and also discuss if further investigation is required to check the possibility of oscillation.

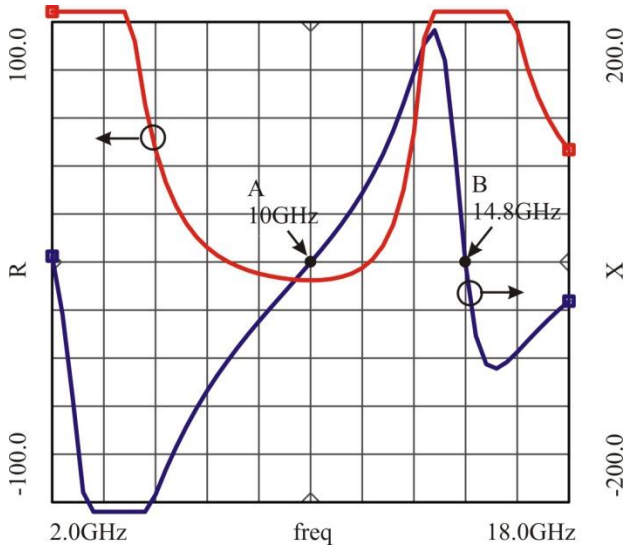

Figure 10E.2 Plot of series impedance oscillation condition

Solution

From the figure, the possible point of series oscillation is point A (10GHz). However, point B (14.8GHz) shows parallel resonance where oscillation is also possible. As previously explained, because the circuit (for which the possibility of parallel oscillation is not known) is investigated for series oscillation, a positive resistance value can appear at the parallel resonant frequency. Thus, a parallel oscillation is possible at a frequency of 14.8 GHz. Therefore, it becomes necessary to obtain the sum of the parallel admittance at this frequency to check the occurrence of parallel oscillation. ■

10.2.1.2 Equilibrium Conditions

In Fig. 10.2, when the equilibrium state is reached, the amplitude of $i(t)$, I_o becomes constant; applying the KVL,

$$\left(Z_A\left(I_o,\omega\right)+Z_L\left(\omega\right)\right)=\left\{R_A\left(I_o,\omega\right)+R_L\left(\omega\right)+j\left(X_A\left(I_o,\omega\right)+X_L\left(\omega\right)\right)\right\}I_o=0 \tag{10.5}$$

and since $I_o \neq 0$,

$$Z_A\left(I_o,\omega\right)+Z_L\left(\omega\right)=R_A\left(I_o,\omega\right)+R_L\left(\omega\right)+j\left(X_A\left(I_o,\omega\right)+X_L\left(\omega\right)\right)=0 \tag{10.6}$$

Rearranging equation (10.6),

$$R\left(I_o,\omega\right)=R_A\left(I_o,\omega\right)+R_L\left(\omega\right)=0 \tag{10.7a}$$

$$X\left(I_o,\omega\right)=X_A\left(I_o,\omega\right)+X_L\left(\omega\right)=0 \tag{10.7b}$$

are the two equations that must be satisfied at equilibrium. The ω_o given by the oscillation start-up condition does not generally satisfy $X_A(I_o,\omega)+X_L(\omega)=0$ in equation (10.7b) at large-signal. Thus, the frequency at equilibrium can be slightly different from the frequency determined at the small-signal oscillation condition. In general however, for high Q, the oscillation frequency is mostly obtained near the frequency determined by start-up. Assuming $X_A(I, \omega_o)$ almost does not vary with the current amplitude I, the amplitude of RF current I_o at equilibrium can be found when the sum resistance R is plotted with respect to the amplitude. Figure 10.7 shows a plot of $R(I,\omega)$ for the current amplitude. In Fig. 10.7, the total resistance value at the small signal is found to be negative. The amplitude of RF current will increase exponentially thereby increasing along the x-axis. Conversely, when the amplitude increases passing through the equilibrium point, since the total resistance value will be positive, the amplitude of RF current decreases exponentially, thereby decreasing along the $-x$ direction. As a result, equilibrium is attained at the point where the total resistance value is 0, i.e., the point where the current amplitude is I_o and thus a steady current amplitude appears.

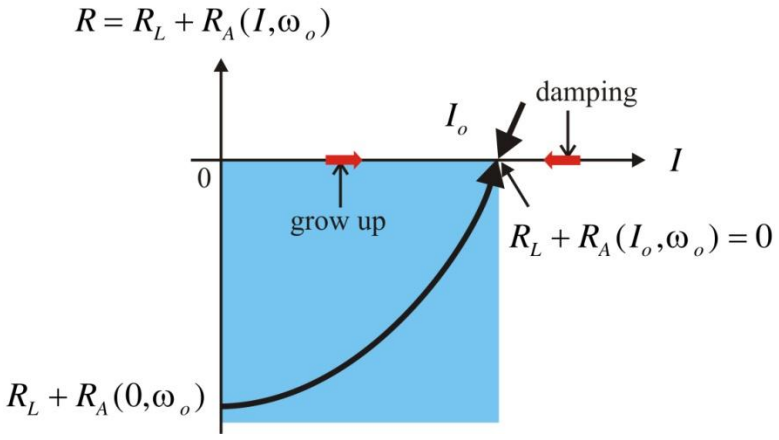

Figure 10.7 Variation of negative resistance with respect to the current amplitude

In addition, the real and imaginary parts of the large-signal admittance equilibrium condition, like the series oscillation circuit, are

$$G_A(V_o,\omega)+G_L(\omega)=0 \tag{10.8a}$$

$$B_A(V_o,\omega)+B_L(\omega)=0 \tag{10.8b}$$

respectively, at which equilibrium can be seen to be attained. Furthermore, the oscillation frequency which determines the attainment of equilibrium by equation (10.8b) is slightly different from the oscillation frequency determined by start-up oscillation condition. To show the equilibrium process, the variation of the total conductance with respect to the amplitude of RF voltage is shown in Fig. 10.8, and similar to series oscillation circuit, equilibrium can be seen to be attained at a voltage of amplitude V_o.

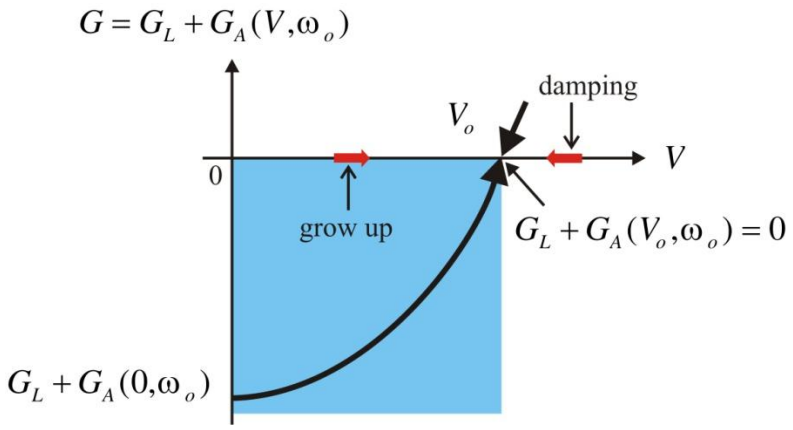

Figure 10.8 Variation of negative conductance with respect to the voltage amplitude

10.2.1.3 Oscillation Start-up and Equilibrium Condition Analysis using ADS

Since it is necessary to calculate the sum of the series impedance in order to simulate a small-signal start-up oscillation condition using ADS, a port is inserted in series between the load and the active part as shown in Fig. 10.9(a) and after the impedance is obtained from one-port S-parameter analysis, the result of $Z_A + Z_L$ at small-signal can be obtained. On the other hand, the result of admittance $Y_A + Y_L$ is obtained by inserting a port in parallel between the load and the active part as shown in Fig. 10.9(b) and performing S-parameter analysis. Thus, to investigate the possibility of oscillation using the admittance or impedance obtained through S-parameters analysis, two S-parameter analyses should be simultaneously performed as shown in Fig. 10.9.

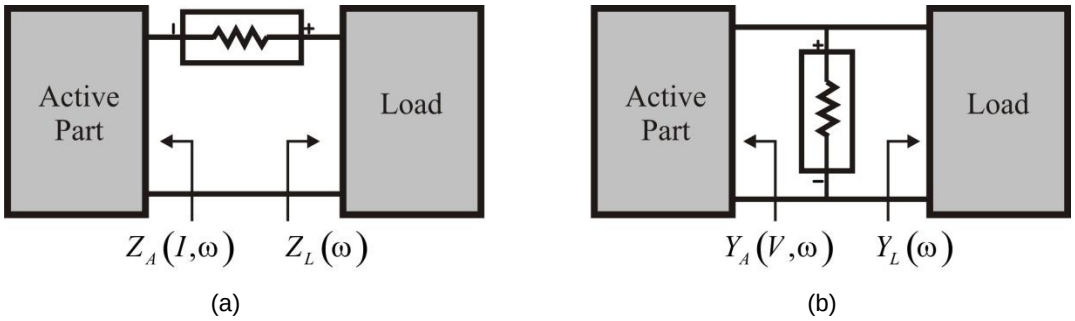

Figure 10.9 Small-signal oscillation simulation: (a) Series and (b) parallel

Next, the large signal equilibrium condition needs to be calculated in ADS in order to determine the exact oscillation frequency and amplitude, which is accomplished by connecting a large signal port as shown in Fig. 10.10 and performing a Harmonic Balance Simulation. For series oscillation, the circuit is connected as shown in Fig. 10.10(a) to determine the equilibrium oscillation point. For parallel oscillation, the circuit is connected as shown in Fig. 10.10(b) to determine the equilibrium oscillation point.

From Fig. 10.10(a), since the sum of the impedances at the series oscillation equilibrium point is 0; the voltage at both ends of the port becomes 0. In that case, the amplitude of the current flowing through the port will just be the amplitude of the current at equilibrium. In contrast, since the sum of the admittance becomes zero at the parallel oscillation equilibrium point, the current

flowing out from the port becomes 0, and thus the amplitude of the voltage across the port will just be the amplitude of the voltage at equilibrium.

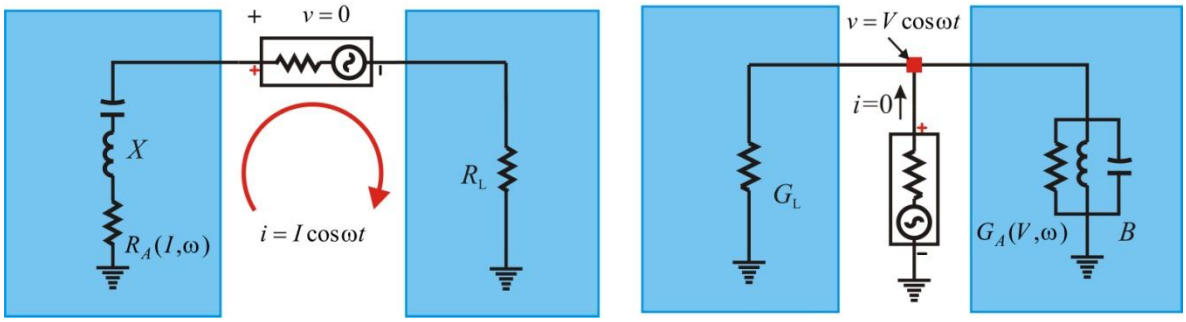

Figure 10.10 Equilibrium point simulation at large-signal

■ Example 10.4

For the nonlinear device represented by the following current-voltage relationship in equation (10E.2), plot the negative conductance, and also by simulation, plot the total conductance when G_L=0.2 as in Fig. 10.8. Furthermore, obtain the voltage when the total conductance is 0, and verify that this is the oscillation output voltage at equilibrium.

$$i = -v + \frac{1}{3}v^3 \tag{10E.2}$$

Solution
When a sinusoidal voltage is applied to the device, the current then is

$$i(t) = -V_p\cos\omega t + \frac{1}{3}\left(V_p\cos\omega t\right)^3 = -V_p\cos\omega t + \frac{1}{3}V_p^3\left(\frac{3}{4}\cos\omega t + \frac{1}{4}\cos 3\omega t\right)$$
$$= -V_p\cos\omega t + \frac{1}{4}V_p^3\cos\omega t + \frac{1}{12}V_p^3\cos 3\omega t$$

Thus, the large-signal conductance becomes

$$G_A\left(V_p\right) = \frac{-V_p + \frac{1}{4}V_p^3}{V_p} = -1 + \frac{1}{4}V_p^2$$

To confirm this by simulation, the device governed by relationship (10E.2) can be configured using SDD (Symbolically Defined Device) as shown in Fig. 10E.3. Furthermore, a parallel resonant circuit resonating at 1 GHz is connected in parallel with the SDD in order to set the oscillation

frequency to 1 GHz. Since the parallel resonant circuit can cause problems at the DC operating point, a DC block is inserted in the parallel resonant circuit of Fig. 10E.3. After such settings and simulation, the following equation is inserted in the Display window to plot the total conductance *G*, the result of which is shown in Fig. 10E.4.

Eqn G=real(I_Probe.i[::,1])/Vac

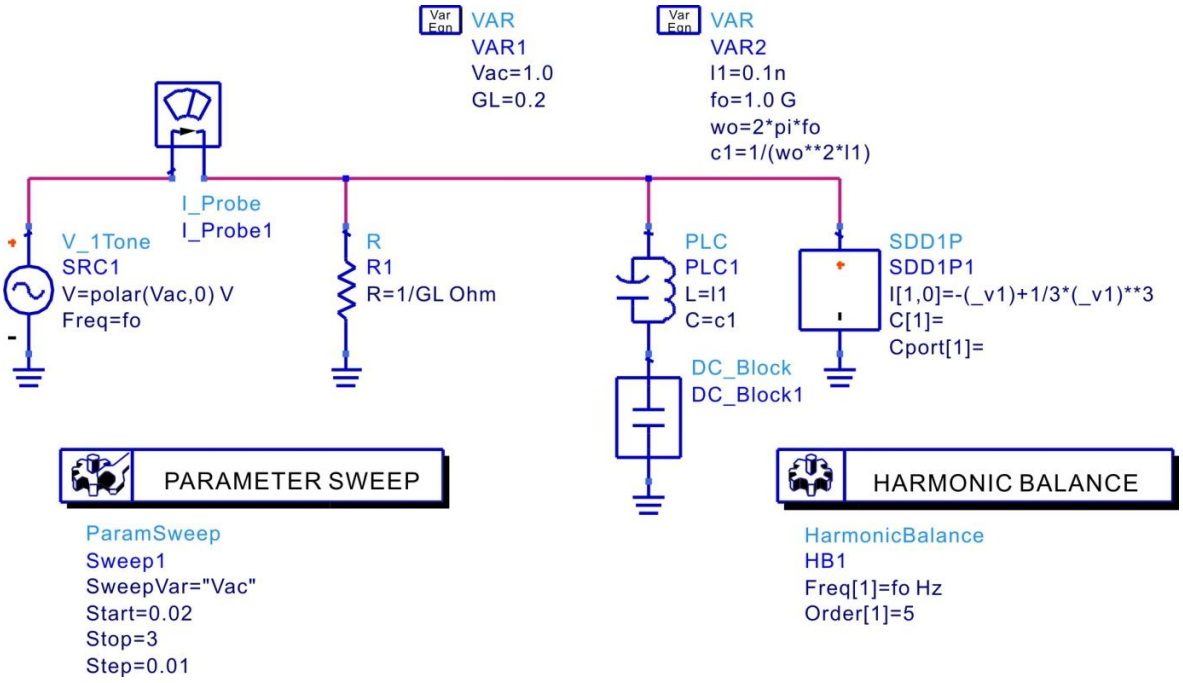

Figure 10E.3 Parallel oscillation circuit

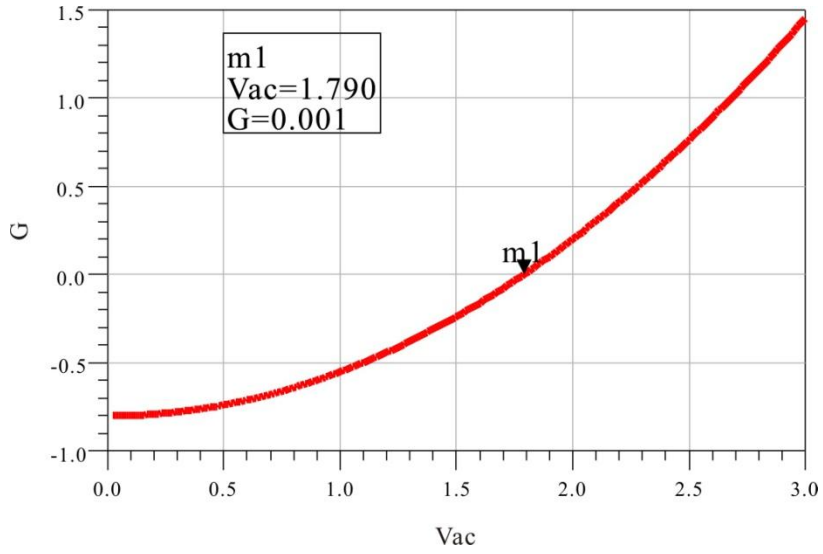

Figure 10E.4 Calculated total negative conductance

The result in Fig. 10E.4 is the same as the theoretically calculated result above, which as can be seen is a parabola. In addition, the point where the current is 0 is the same point where the total conductance is 0 and the amplitude of the voltage can be seen to be approximately 1.8 V. To confirm this, **OscPort** which will be explained in the next section can be used to verify the output oscillation at equilibrium. The output at oscillation equilibrium can be known by setting up the schematic as shown in Fig.10E.5 and simulating. The result is shown in Fig. 10E.6. The waveform in Fig. 10E.6, which is in the form of a sinusoidal waveform, shows a significant amount of distortion due to harmonics, but the amplitude of the oscillation waveform can be seen to be approximately 1.8 V.

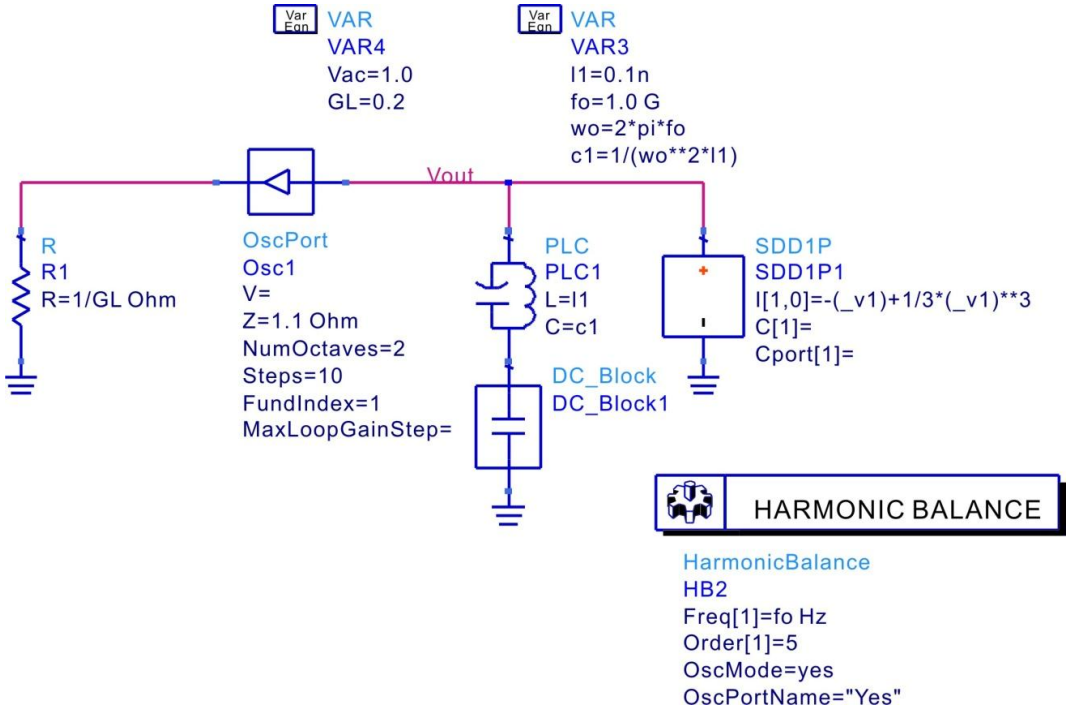

Figure 10E.5 Schematic for obtaining the waveform of the parallel oscillation circuit

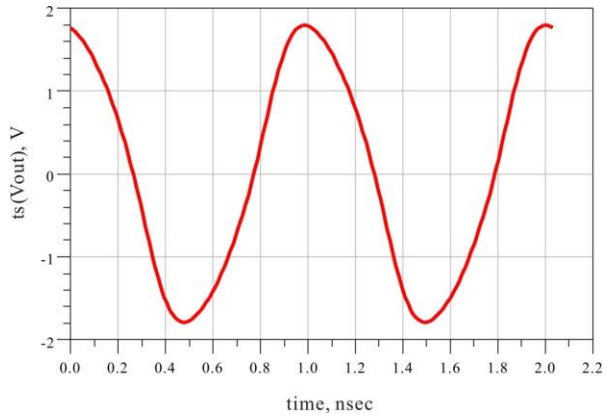

Figure 10E.6 Calculated oscillation waveform

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10.2.2 Oscillation Conditions Based on Reflection Coefficient

10.2.2.1 Start-up and Equilibrium Conditions Based on Reflection Coefficient

Oscillation condition based on reflection coefficient is widely used as it is easier to measure reflection coefficient at high frequencies compared to the measurement of impedance. This is similar to the oscillation condition based on one-port impedance discussed earlier. In Fig. 10.11, the reflection coefficients of the active part and load are defined for the same reference impedance Z_o, and their 1-port reflection coefficients are Γ_A and Γ_L respectively. Also, the impedances corresponding to these reflection coefficients are denoted by Z_A and Z_L respectively.

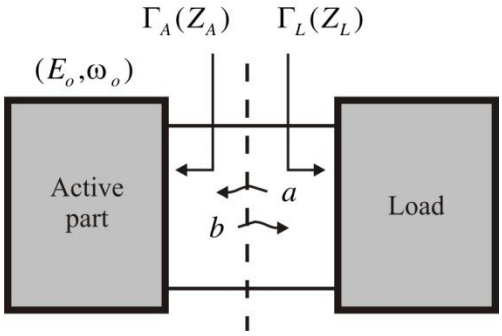


Figure 10.11 Oscillator circuit defined based on Reflection Coefficient

When the incident voltage $a=E\bullet\cos\omega t$ corresponding to the available power of $P_A = E^2$ is applied from the load, the new reflected voltage from the load a' after a round-trip between the active part and load is

$$a' = \Gamma_L(\omega)\Gamma_A(E,\omega)a \tag{10.9}$$

The reflected voltage a' becomes a new incident voltage which again makes a round trip between the active part and load. Thus, for exponential growing, the following start-up conditions must be satisfied:

$$\left|\Gamma_L(\omega_o)\Gamma_A(0,\omega_o)\right| > 1 \tag{10.10a}$$

$$\angle\Gamma_L(\omega_o)\Gamma_A(0,\omega_o) = 0, \tag{10.10b}$$

where $\Gamma_A(0,\omega_o)$ represents the small-signal reflection coefficients of the active part. Equation (10.10a) is the condition that must be satisfied for the signal to grow through the repetition of round-trips, while equation (10.10b) is the condition requiring that the phase remains unchanged when such round-trips continue repeatedly.

In addition, for this oscillation condition to be stable, the slope of equation (10.10b) for the frequency must be negative. That is

$$\frac{\partial\angle\Gamma_L(\omega_o)\Gamma_A(0,\omega_o)}{\partial\omega} < 0 \tag{10.11}$$

The example of oscillation condition satisfying (10.10) and (10.11) is shown in Fig. 10.12. The magnitude and phase of $\Gamma_A\Gamma_L$ that satisfy the oscillation condition are plotted in Fig. 10.12. From Fig. 10.12, it can be found why the condition in (10.11) is necessary. When the frequency is lower than the oscillation frequency, a positive phase occurs, and by repeated round-trips, the frequency increases as the phase continues to increase, eventually approaching the oscillation frequency. In contrast, when the frequency is higher than the oscillation frequency, the phase becomes negative and by repeated round-trips, the phase decreases continuously and eventually attains equilibrium at the frequency of oscillation. Thus, equation (10.11) provides a stable oscillation.

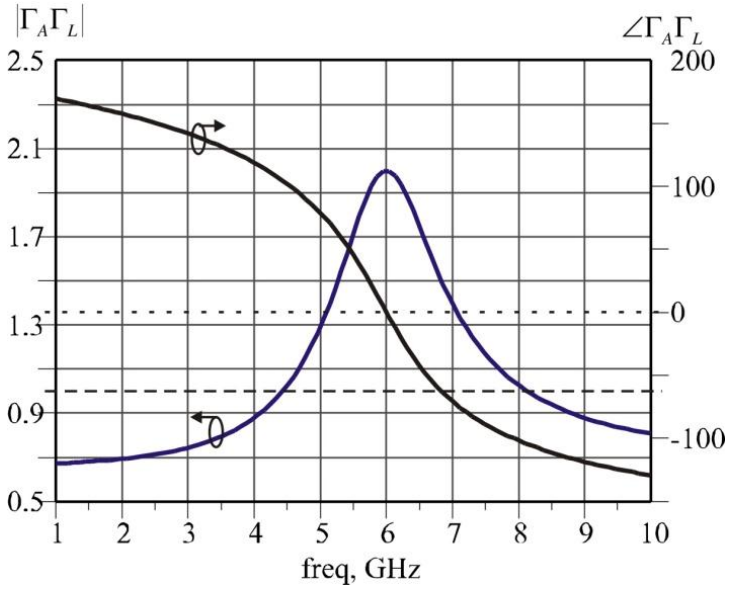


Figure 10.12 Plot of $\Gamma_L\Gamma_A(0,\omega_o)$

It must be noted that the oscillation condition given by equation (10.10) obviously guarantees oscillation. However, oscillation can also occur under other conditions and thus the conditions given by equation (10.10) are the sufficient conditions for oscillation. Furthermore, this condition changes when the reference impedance used to measure the reflection coefficients of the active part and load changes. This is summarized in the Appendix E.

The plot of $\Gamma_L\Gamma_A(E,\omega_o)$ for E is as shown in Fig. 10.13. Similar to impedance oscillation conditions described earlier, E will grow exponentially at small-signal because $\Gamma_L\Gamma_A(E,\omega_o)>1$ and increases along the x-axis, while it progresses in the decreasing direction when E becomes greater than E_o. Therefore, at equilibrium,

$$\left|\Gamma_L(\omega_o)\Gamma_A(E_o,\omega_o)\right| = 1 \tag{10.12a}$$

$$\angle\Gamma_L(\omega_o)\Gamma_A(E_o,\omega_o) = 0, \tag{10.12b}$$

In other words, at the equilibrium point, the magnitude of the product of the reflection coefficients due to round-trip is 1, and its phase is 0°.

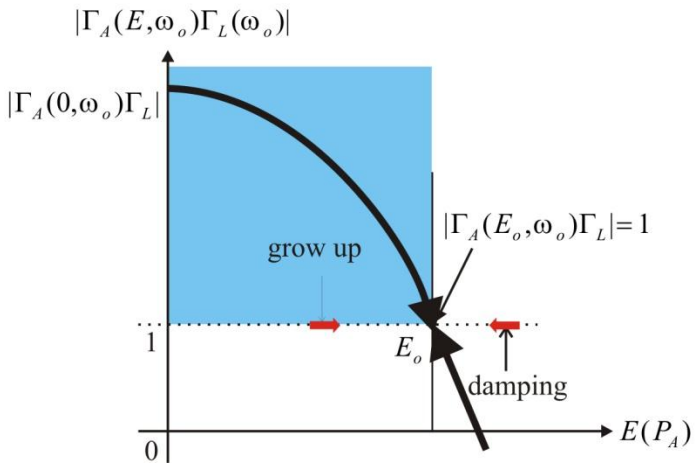


Figure 10.13 Variation of $\Gamma_A\Gamma_L$ with respect to the power

10.2.2.2 Circuit Implementation

The oscillation condition based on the reflection coefficient described above can be implemented using a circulator as shown in Fig.10.14.

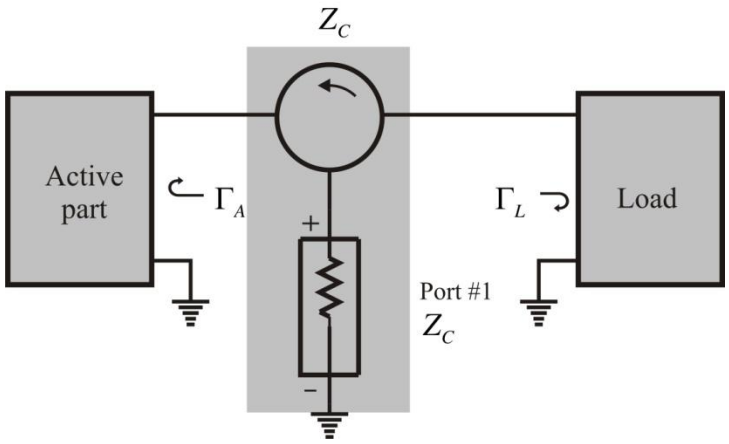


Figure 10.14 Measurement of $\Gamma_A\Gamma_L$

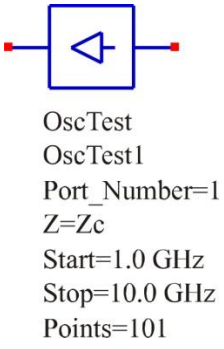


Figure 10.15 OscTest in ADS

As shown in Fig. 10.14, when the load and active part are connected to a broadband circulator with the same reference impedance as the Port, the reflection coefficient S_{11} at the port can be expressed as $S_{11}= \Gamma_A\Gamma_L$. Note that the product of the reflection coefficients $\Gamma_A\Gamma_L$ is thus measured at the reference impedance Z_c of the port and as a result, different port reference impedance will result in different value of $\Gamma_A\Gamma_L$. The oscillation condition is thus specified under the reference impedance Z_c. The circulator and port in the shaded box shown in Fig. 10.14 is already implemented as **OscTest** in ADS, and this is shown in Fig. 10.15. Z in Fig. 10.15 represents the reference impedance of the port and $\Gamma_A\Gamma_L$ is computed for the frequency range which is specified as **Start** and **Stop**.

■ Example 10.5

The following is a small-signal series oscillation circuit. The reference impedance of **OscTest** is set to100ohm, Calculate $\Gamma_A\Gamma_L$.

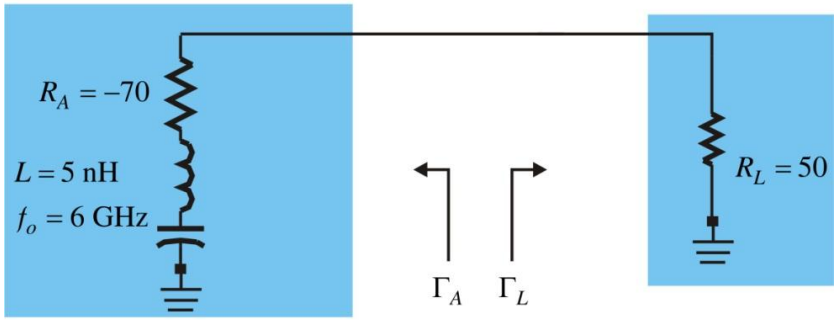


Figure 10E.7 Small signal series oscillation circuit

Solution

OscTest shown in Fig. 10E.8 is inserted in the circuit to calculate mag(S_{11}) and $\angle S_{11}$. The results are shown in Fig. 10E.9.

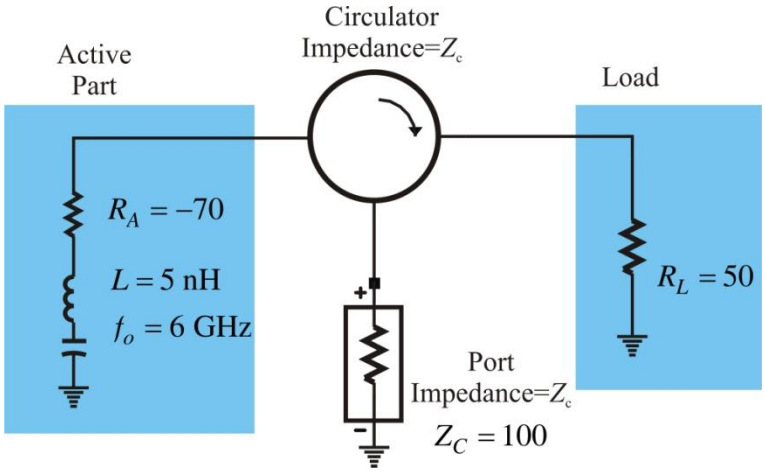


Figure 10E.8 Oscillation condition computation using **OscTest**

Calculating the product of the reflection coefficients at the oscillation frequency,

$$\Gamma_A\Gamma_L = \frac{-70-100}{100-70}\times\frac{50-100}{50+100} = 1.88,$$

which can be seen to be the same as the results shown in Fig. 10E.9. In this figure, the magnitude of $\Gamma_A\Gamma_L$ at the point where oscillation occurs is greater than 1, and the phase can be seen to be 0°. Furthermore, the phase slope with respect to frequency can be seen to be negative.

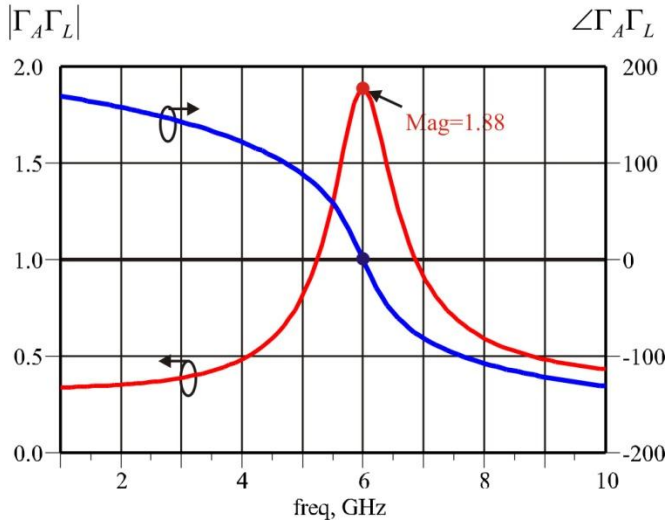


Figure 10E.9 Oscillation condition computed using **OscTest**

Notably, the reference impedance of the reflection coefficient is set to 100 ohm as 50 ohm reference impedance makes $\Gamma_A\Gamma_L$=0 which means, the above oscillations condition will not be satisfied. However, this is the oscillation condition variation based on reference impedance change and this circuit clearly oscillates. Therefore, selecting appropriate reference impedance makes it easy to check the oscillation condition. For more information, refer to the Appendix E.

■

10.2.2.3 Equilibrium Based on Reflection Coefficient

The start-up oscillation condition based on the reflection coefficient can be applied to derive the large-signal equilibrium conditions. That is, irrespective of parallel or series oscillation, the product of the reflection coefficients $\Gamma_A\Gamma_L$ must be 1 at equilibrium. Denoting the available power from the port as P_a, since the power delivered to the oscillator circuit from the port through the circulator is $P_a(1-|\Gamma_L\Gamma_A|^2)$, it should be 0 at equilibrium. Thus, when the power available from the port is increased, the port delivers no power to the oscillator circuit at equilibrium. The delivered power is mag(V*I) as shown in Fig. 10.16. Therefore, after finding this port voltage and current where the delivered power becomes 0, every voltage and current in the oscillator circuit at equilibrium can be obtained by calculating the currents and voltages of the oscillator circuit at this port power.

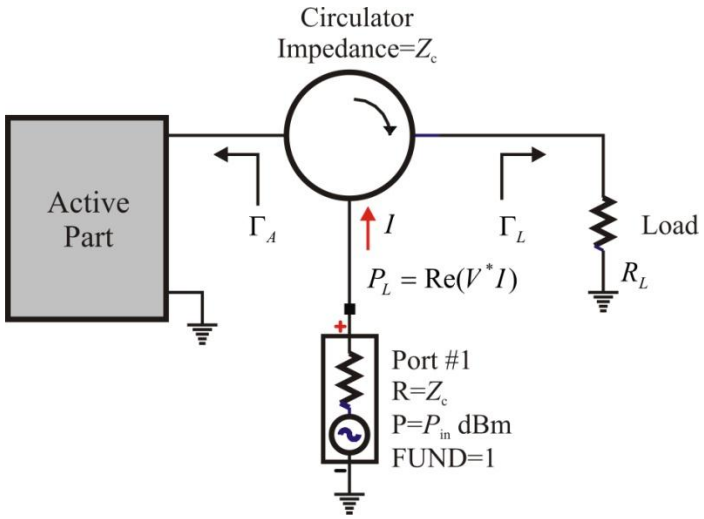


Figure 10.16 Large-signal equilibrium point in oscillator

Thus, to determine the large-signal equilibrium state using the reflection coefficient, the power of the port is increased where the large signal reflection coefficient becomes equal to 1. Then, using the obtained port power and frequency, every current and voltage of the oscillator circuit can be calculated, which in turn can be used to determine the waveforms of every node in the oscillator circuit at equilibrium. These operations can be performed automatically in ADS which is usually done using the **OscPort**. That is, by performing the simulation using this **OscPort** in conjunction with the **HB simulator** (*i.e.* a simulation in which the large signal available power of the port is varied to determine the oscillation power and frequency at equilibrium), the oscillation output at equilibrium can be obtained. This is shown in Fig. 10.17. Figure 10.17(a) shows the concept of **OscPort** analysis in ADS. The oscillation output at equilibrium can be obtained by using the **HB simulator** together with the circuit shown in Fig. 10.17(a).

The *Z* of the **OscPort** in Fig 10.17(b) is the reference impedance of the circulator and port. Since the oscillation frequency at equilibrium differs from the estimated small-signal oscillation frequency, **NumOctaves** is specified to determine the frequency tuning range at a frequency range corresponding to 0.5 to 2 times the estimated frequency. Furthermore, **FundIndex** is the specified estimated oscillation frequency in the **HB simulator**. It represents simulation for the fundamental frequency which in most cases is 1.

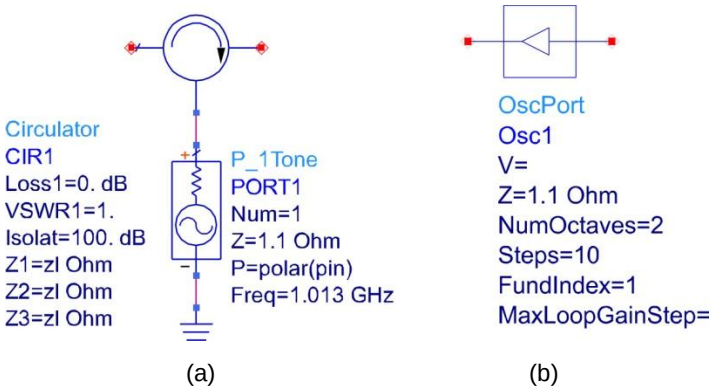
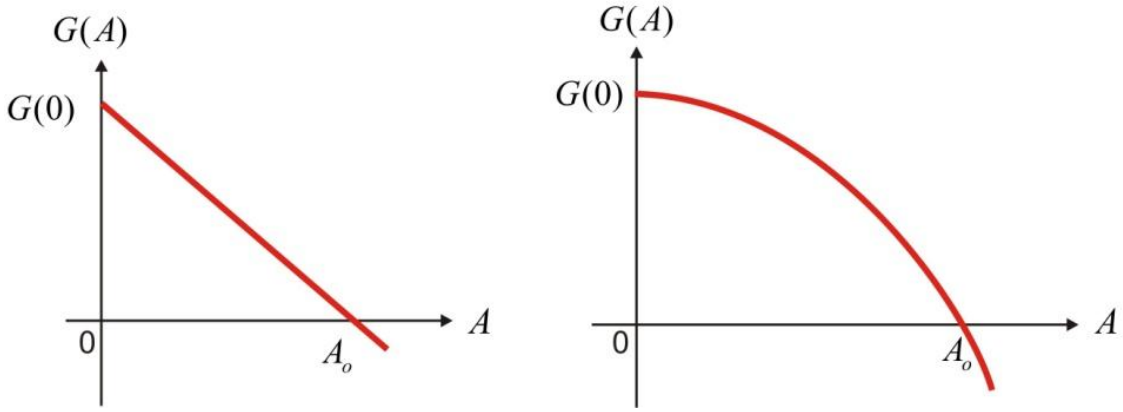


Figure 10-17 (a) Equivalent circuit of the **OscPort** and (b) **OSCPORT**

■ Example 10.6

When the diode admittance is denoting as Y_A=–$G(A)$+$jB(A)$, given that one admittance has the real part decreasing linearly with the amplitude as $G(A) = g(0)–k_1A$ as shown in Fig. 10E.10(a) and that the other has the real part decreasing as $G(A) = g(0)–k_1A^2$.



(a) (b)

Figure 10E.10 G(*A*) with respect to voltage amplitude: (a) Linear decrease and (b) quadratic decrease

The load values giving maximum oscillation output power are known to be 1/3•$G(0)$ and 1/2•$G(0)$, respectively. In Example 10.4, the negative conductance is $G(A)=1-1/4A^2$. Thus, it delivers the maximum oscillation output power to the load when the load conductance G_L is equal to 0.5. Confirm this through simulation and calculate the maximum oscillation output power.

Solution

As mentioned earlier, the maximum oscillation power occurs at G_L=0.5 and since the amplitude at equilibrium must satisfy

$$-G(A)+G_L=-1+\frac{1}{4}A^2+\frac{1}{2}=0,$$

it can be seen that, $A=(2)^{½}$. Thus, the maximum output is

$$P_{L\max}=\frac{1}{2}G_LA^2=\frac{1}{4}\times 2=0.5\ (\text{W})$$

To confirm the oscillation output power for this load G_L, Harmonic Balance Simulation is performed using **OscPort** as shown in Fig. 10E.11. After simulation, the equation shown below is inserted in the Display window to calculate the output P_L due to the load G_L

Eqn PL=1/2*GL*mag(Vout[::,1])**2

This result is shown in Fig. 10E.12. As expected, the maximum output is 0.5 W.

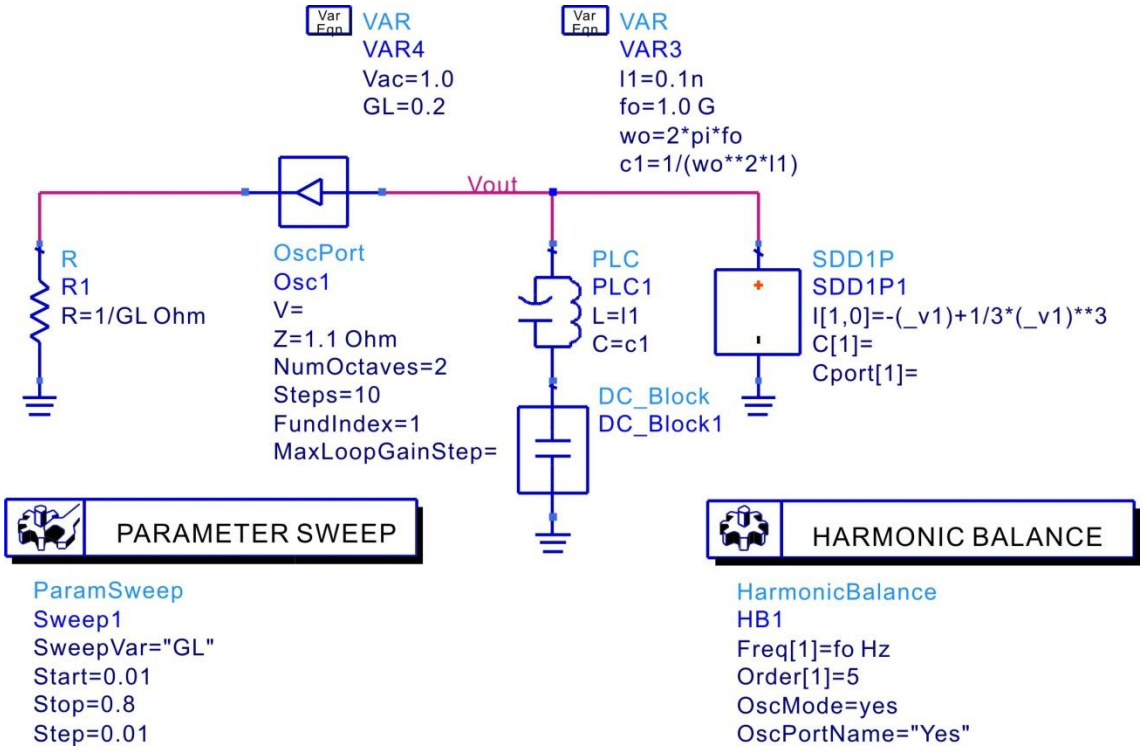


Figure 10E.11 Schematic for obtaining the oscillation output power for the variation of G_L

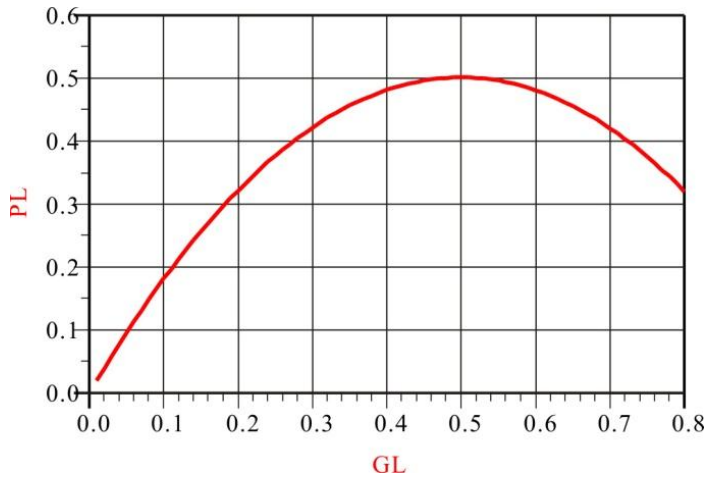


Figure 10E.12 Oscillation Output power for G_L change

■

10.2.3 Start-up and Equilibrium Conditions Based on Open-Loop Gain

The one-port oscillation condition described earlier using impedance and reflection coefficient is a direct method for oscillator circuits employing diodes, but not so for the analysis of oscillator circuit

using transistors. Transistors are mostly used as amplifiers and are configured as oscillators using feedback network. 1-port analysis is limited when it comes to analyzing oscillators employing such feedback network, making it difficult to understand the role of the feedback network. In an oscillator using this feedback, rather than reflection coefficient or impedance, the use of open-loop gain makes the understanding of oscillators employing transistors easy, and the description of the maximum output power condition of the oscillator or phase noise becomes easy. However, in high-frequency, it is generally difficult to calculate the open-loop gain due to the bi-directional properties of transistors, which cannot be unilaterally approximated unlike in low frequency circuit. In this case, the accurate open-loop gain cannot be calculated by approximation in the direction of power delivery. Recently published papers [1], [2], have theoretically revisited the calculation of this open-loop gain, transistor oscillator design using this method are expected to be widely used.

10.2.3.1 Start-up and Equilibrium Conditions Based On Open-Loop Gain

Figure 10.18 is a form of oscillator configuration in which the output of the amplifier employing a transistor is fed back through a resonator. Here, the feedback loop is broken, which is done to obtain the open-loop gain. In the figure, the gain of the amplifier can be considered to be varying with the amplitude of the input signal A, and the transfer function of the resonator can generally be expressed as in equation (10.13).

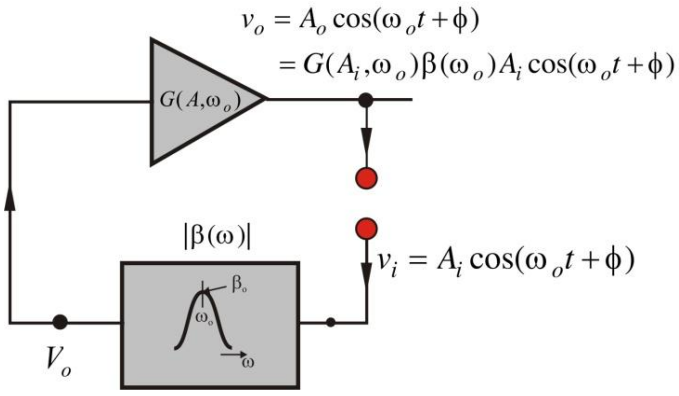


Figure 10.18 Oscillators configuration with feedback

$$\frac{V_o}{V_i} = \frac{\beta_o}{1 + jQ_L\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)}, \tag{10.13}$$

where $ß_o$ is the transmission coefficient at the resonant frequency ω_o, and Q_L represents the loaded Q of the resonator.

The open-loop gain $L(A, \omega)$ is defined as

$$L(A,\omega) = G(A,\omega)\beta(\omega) \tag{10.14}$$

which is the output voltage per loop trip of the input signal. The typical small-signal open-loop gain $L(0,\omega)$ is shown in Fig. 10.19.

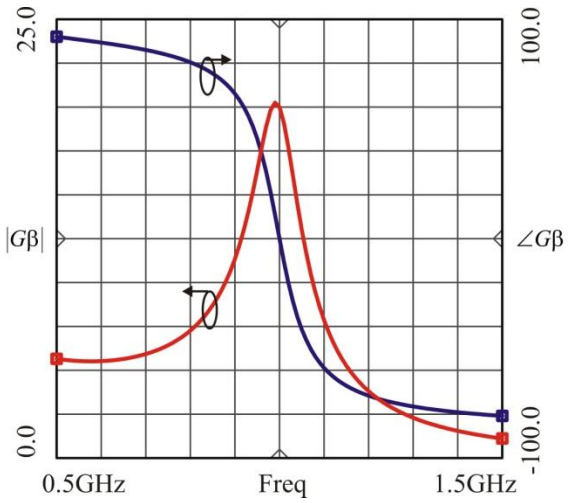


Figure 10.19 The frequency characteristics of the small-signal open loop gain

Because the gain $G(0,\omega)$ is almost constant, the shape of the open loop gain with frequency generally resembles the frequency response of the resonator given by equation (10.13). The maximum value of the open loop gain occurs at the resonant frequency ω_o and decreases below and above the resonant frequency as shown in Fig. 10.19. Furthermore, the phase response can be seen to be 0° at the resonant frequency, and the phase approaches 90° below the resonant frequency while it approaches –90° above the resonance frequency.

When a sinusoidal input $A\bullet\cos(\omega_o t)$ having the resonant frequency is applied to the input of Fig. 10.18, a signal $L(A,\omega_o)\bullet A\cos(\omega_o t)$ appears at the output of the amplifier. It must be noted that, the output of the loop has the same phase as the input and only the amplitude varies. This output is again repeatedly applied to the input of Fig 10.18 when the loop is closed. When the loop gain $L(A,\omega_o) > 1$, the amplitude grows larger after every trip of feedback loop. Therefore, in order for the signal to grow at small-signal, $L(A,\omega_o) > 1$ at the frequency ω_o with the phase 0° and oscillation can then be formed. This is called the *Barkenhausen Criterion.* That is, when the following conditions are satisfied, the amplitude grows by repeated feedback and oscillation can occur.

$$\angle L(0,\omega_o) = 0 \tag{10.15a}$$

$$\left|L(0,\omega_o)\right| > 1 \tag{10.15b}$$

$$\left.\frac{\partial \angle L(0,\omega_o)}{\partial \omega}\right|_{\omega=\omega_o} \tag{10.15c}$$

The frequency response characteristics shown in Fig. 10.19 can be seen to satisfy the conditions of equation (10.15).

The reason equation (10.15c) must be satisfied is that, when the frequency is lower than the resonant frequency, the phase of the loop gain in Fig 10.19 becomes positive, and thus the phase grows positively for every trip of the loop. This continuous increase in the phase represents an increase in frequency, eventually approaching the resonant frequency. In contrast, when the

frequency is higher than the resonant frequency, the phase of the open loop gain in Fig. 10.19 becomes negative and reduces negatively for every trip of the loop and the continuous decrease in phase represents a decrease in frequency and thus approaches the resonant frequency. On the other hand, when the phase response of the open loop gain is opposite to that given by equation (10.15c), even when there is a small phase jitter, it will be away from the resonance frequency, and oscillation will not occur. Thus, equation (10.15c) is an important criterion in determining the occurrence of oscillation.

Furthermore, the variation of the loop gain according to the amplitude is plotted as shown in Fig 10.20. For small signals ($A \cong 0$), as the magnitude of the open loop gain is greater than 1, the amplitude increases exponentially. Increasing in the direction of A-axis causing the loop gain to reduce. In contrast, when the amplitude is greater than the equilibrium point, the amplitude reduces, resulting in a decrease in the direction of $-A$ axis. Eventually, the amplitude A reaches A_o at the point where the open loop gain is 1. Therefore, the oscillation frequency is determined by

$$\angle L\left(A_o, \omega_o\right) = 0, \tag{10.16}$$

And the oscillation amplitude A_o is determined by the following equation,

$$\left|L\left(A_o, \omega_o\right)\right| = 1 \tag{10.17}$$

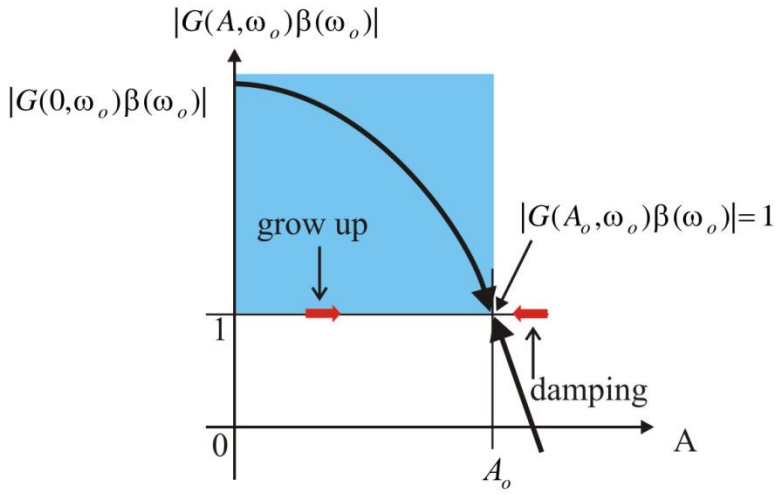


Figure 10.20 Variation of the open loop gain with amplitude

10.2.3.2 Open Loop Gain

Open-loop gain is obviously more natural and easier to apply in determining the oscillation condition for an oscillator circuit configured using feedback circuit, compared to the one-port method. The previous amplifier obviously can be composed of transistor while the feedback circuit provides the condition necessary for such transistor to oscillate. The oscillator circuit using such feedback can be represented conceptually as shown in Fig. 10.21(a). In order to calculate the open-loop gain of this circuit, the circuit is cut to break up the feedback as shown in Fig. 10.21(b). The open loop gain can be computed by applying a test source V_t and finding the resulting return voltage

V_r at the load having the impedance Z_t looking into the source side prior to breaking the loop. However, it is generally not easy to find the impedance Z_t at the cut plane. Rather, the broken feedback circuit of Fig. 10.21(b) is defined as a new two-port circuit, and the load impedance Z_t can be considered as the impedance looking into the circuit which is composed of an infinite number of the newly defined 2-port circuit connected in cascade. This way, the small-signal open-loop gain can be expressed in terms of the 2-port S-parameters for the newly defined 2-port circuit as

$$L(\omega) = \frac{S_{21} - S_{12}}{1 - S_{11}S_{22} + S_{21}S_{12} - 2S_{12}} \tag{10.18}$$

Thus, the circuit oscillates when the calculated open-loop gain in equation (10.18) satisfies the oscillation condition in equation (10.15).

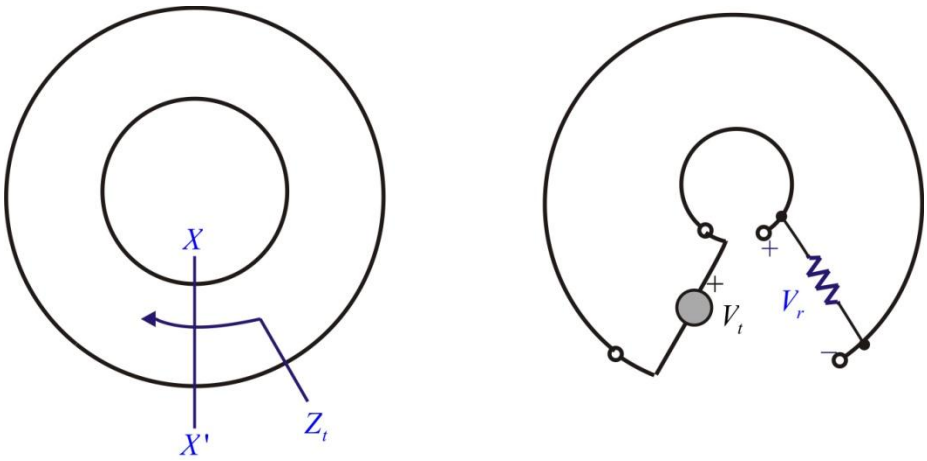


Figure 10.21 (a) Feedback circuit and (b) circuit for calculating open-loop gain

In equation (10.18), when S_{11}, S_{22}, and S_{12} are small, the loop gain is simplified as follows:

$$L(\omega) \cong S_{21} \tag{10.19}$$

Thus from equation (10.19), the oscillation condition is determined as follows:

$$dB(S_{21}) \geq 0 \tag{10.20a}$$

$$\text{phase}(S_{21}) = 2n\pi \ (n=0,1,2,3\cdots) \tag{10.20b}$$

The feedback type oscillator can easily be designed using the equations in (10.20). The feedback type oscillator is conventionally composed of the cascade connection of 2-port circuits. For example, the oscillator circuit in Fig. 10. 18 can be viewed as the cascade connection of amplifier and feedback resonator. Using the S-parameters of each block of the oscillator circuit, the 2-port S-

parameters of the open loop can be obtained. Also, if each block is matched, the open loop gain is simply the product of S_{21} of each block and the oscillation frequency satisfying (10.20) can be easily found. Once the open loop satisfying equation (10.20) at the oscillation frequency is obtained, the oscillator can simply be configured by closing the open loop. In addition, the large-signal equilibrium conditions can be obtained from the response of the open-loop gain for amplitude change, which is computed using **OscPort** in ADS.

■ Example 10.6

The circuit shown below is a Colpitts oscillator. Calculate its oscillation frequency by the open-loop gain method using ADS.

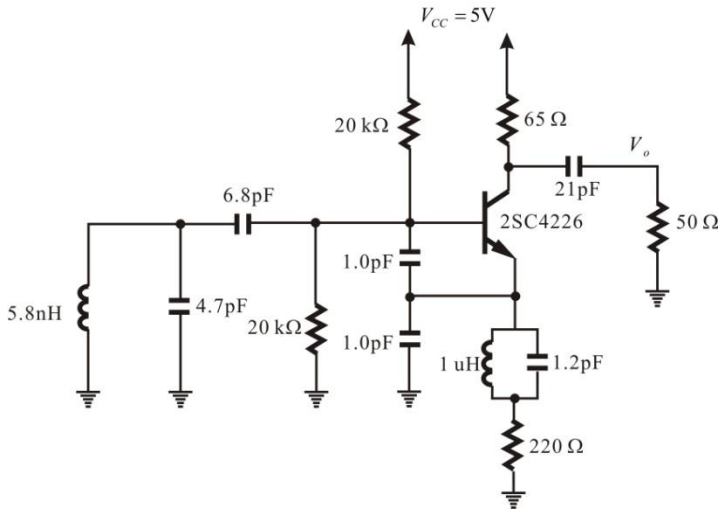


Figure 10E.13 Colpitts Oscillator Circuit

Solution

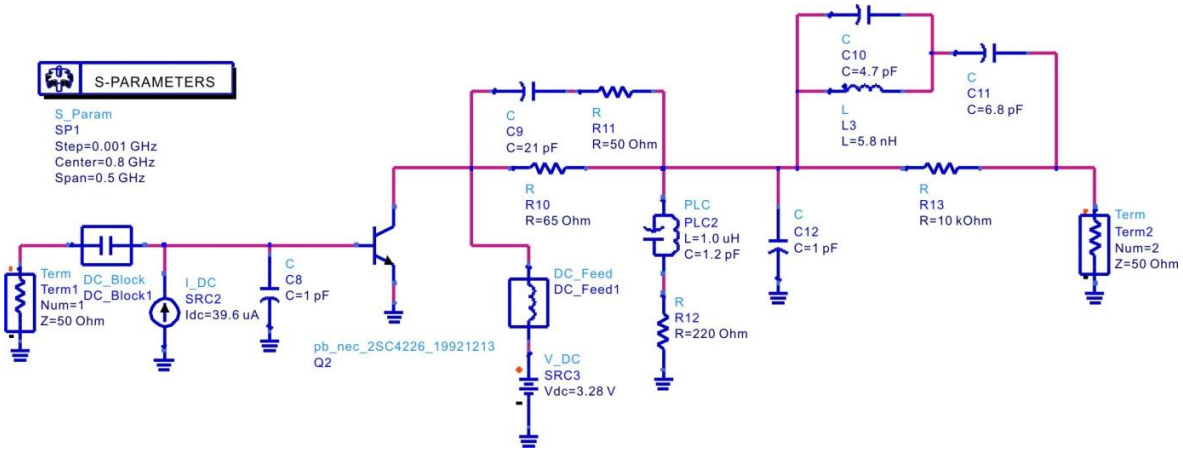


Figure 10E.14 Circuit for calculating the open loop gain

In the circuit of Fig. 10E.13, the ground point is eliminated and a new ground point is set at the emitter of the transistor. With the changed ground point, the input of the open loop is defined between the base-emitter of the transistor and the open loop is formed by breaking the oscillator circuit as shown in Fig.10E.14. In order to maintain the DC operating point of the transistor, collector-emitter voltage and base current are determined through DC simulation in advance for the circuit in Fig. 10E.13 and the collector-emitter voltage and base current are supplied by a DC current source and a voltage source as shown in Fig. 10E.14. After setting up the circuit as such, S-parameter simulation is carried out.

In order to compute and plot the open-loop gain after simulation, the following equation is inserted in the Display window.

Eqn G=(S(2,1)-S(1,2))/(1-S(1,1)*S(2,2)+S(1,2)*S(2,1)-2*S(1,2))

The results are shown in Fig. 10E.15; the oscillation frequency can be seen to be approximately 827 MHz. In order to investigate the large-signal oscillation frequency, **OscPort,** described previously, is inserted in the oscillator circuit to calculate the oscillation frequency. The calculated result confirms the obtained 827 MHz shown in Fig. 10E.15.

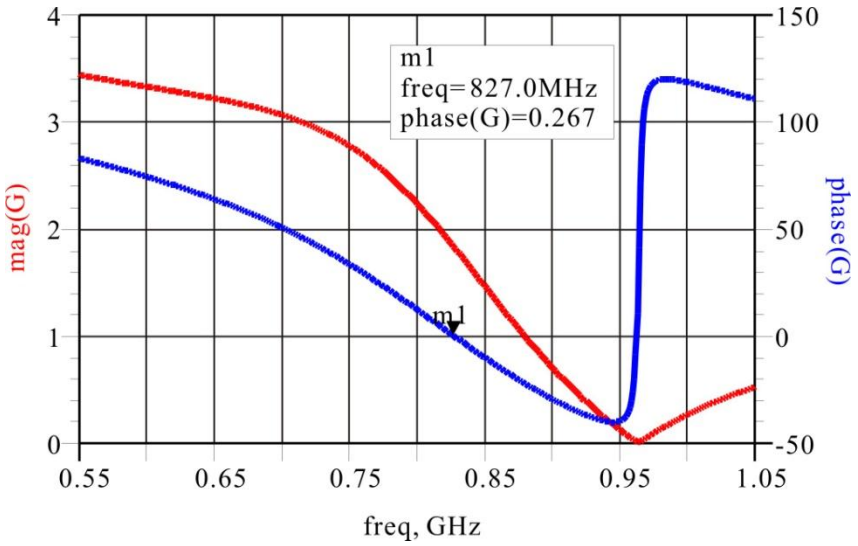


Figure 10E.15 Open-loop gain calculation

Notably, the ground point was moved to the emitter of the transistor for the calculation of the open-loop gain, which made the calculation easy. Such change of the ground point is frequently used in oscillator design and is called *virtual ground technique*.

■

10.3 PHASE NOISE

10.3.1 Spectrum of Oscillation Waveform

The typical output waveform of an oscillator is not a pure sine wave, its amplitude and phase fluctuates with time. Thus, denoting the oscillation output power across the convenient 1 ohm resistor as *C*, the waveform can be expressed in time domain as:

$$v(t) = \sqrt{2C} \cdot \left(1 + a(t)\right) \cos\left(\omega_o t + \phi(t)\right), \tag{10.21}$$

where $a(t)$ represents the fluctuation of the amplitude in time domain, which is called the Amplitude Modulation (AM) noise of the oscillator. Conversely, $\phi(t)$ is called the phase noise due to fluctuation of the oscillation output phase. Two major issues associated with the understanding of this noise. The first is the mathematical model or mechanism of the amplitude and phase noises and the second is how to measure such noises. We first discuss the measurement method and then the mathematical model of the phase noise.

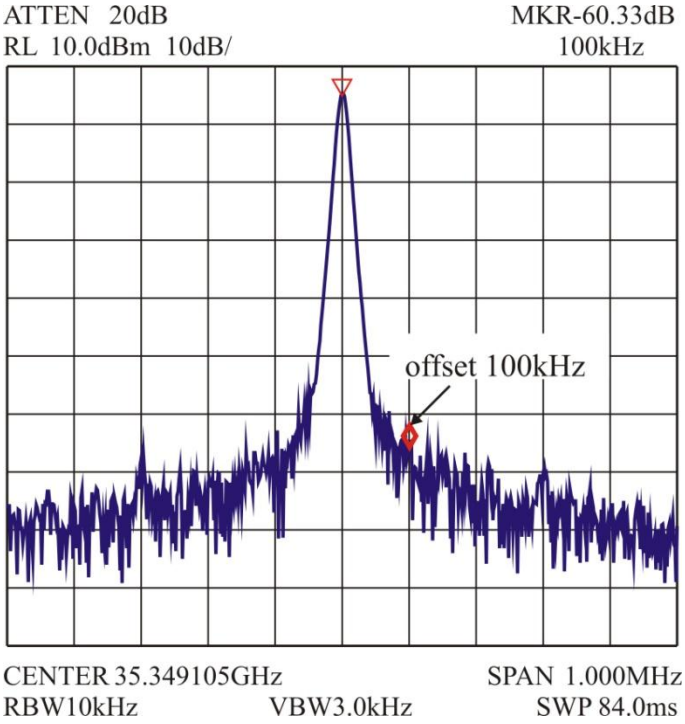


Figure 10.22 Spectrum of oscillator output waveform

When the waveform represented by equation (10.21) is observed on a spectrum analyzer, the spectrum is usually as shown in Fig. 10.22. The spectrum analyzer can simply be thought of as equipment showing the filtered output for a periodical input. The filter in the spectrum analyzer moves the center frequency with time while maintaining the user–specified resolution bandwidth (RBW). Thus, the spectrum analyzer shows the power within the RBW for frequency. In displaying, the spectrum analyzer averages the measured power within the RBW in a given amount of time. VBW (Video Bandwidth) is used as a measure of time averages. Usually because VBW is expressed as frequency, it is the reciprocal of the average time and so it is smaller than the RBW. The spectrum of Fig. 10.22 was measured for a span of 1MHz at the center frequency of 35.349 GHz. Also, RBW = 10 kHz and VBW = 3 kHz. Thus, the spectrum of Fig. 10.22 represents average power in the 10 kHz bandwidth over 1/3 msec.

Furthermore, when equation (10.21) is expanded, it can be considered as the superposition of sinusoidal component of frequency ω_o, whose power is C, and a noise power. The sine wave power, from the results of Fig. 10.22, appears as the power of the center frequency component and the noise power has a distribution which is spread around the center frequency. Since the spectrum of the sinusoidal wave of frequency f_o has the spectrum of $\delta(f–f_o)$, a power C of the sine wave appears when f_o within RBW, otherwise 0. In addition, the value of the sinusoidal power C does not change even when RBW is changed; that is, whether RBW is lowered or increased, the same power appears. On the other hand, it should be noted that noise density (noise power per bandwidth) is constant in the case of the noise. Thus, lowering RBW, the power measured within RBW is lowered, whereas the power measured within RBW is raised when RBW is increased.

■□ Example 10.7

In Fig. 10.22, the ratio of the center frequency power (or the carrier power) to noise power at an offset of 100 kHz from the center frequency is measured to be about –60.33dBc. Calculate the carrier to noise power ratio measured at a 100 kHz offset when the RBW is changed to 1 Hz. Furthermore, also calculate the power when the RBW is changed to 1 kHz.

Solution

As the power of the center frequency is the sine wave power, it does not change even if RBW is changed. However, the power at 100 kHz offset is a noise power and thus changes when RBW is changed. Since the power is –60.33 dB when RBW = 10 kHz, then –60.33 dB/10 kHz = -100.33 dB/Hz. In addition, when the RBW is changed to 1 kHz, the power at the Marker by the same method can be seen to be –70.33 dB.

■

The spectrum of Fig. 10.22 can be seen as representing the contribution of a sine wave output and noise. Also the noise power comes from the combined effect of fluctuations in the amplitude and the phase. However, for most oscillators, because the fluctuation effect coming from the amplitude is low compared to that coming from the phase, the spectrum above is mostly known to occur due to phase fluctuation.

The following conceptual experiment can be thought of as the proof for the above claim. That is, in order to eliminate the AM noise due to fluctuation in the amplitude, the oscillator output is passed through a limiter and then passing the output through a narrow bandwidth bandpass filter to remove harmonics. The resulting spectrum reflects the phase fluctuation alone. However, in most cases, almost the same spectrum is obtained as a result of this experiment, which leads to the conclusion that, the above spectrum is known to be mostly due to the phase noise. In addition, because the AM noise can always be removed using the same method, the spectrum above can be considered to represent the phase noise.

10.3.2 Relationship between Phase Noise Spectrum and Phase Jitter

To see the relationship between the spectrum shown in Fig. 10.22 and the phase fluctuation, consider a part of the noise spectrum at a frequency offset of ω_m from the center frequency and the sine wave output as shown in Fig. 10.23. The waveforms of which in the time domain can be expressed as

$$v(t) = \sqrt{2C}\cos(\omega_o t) + \sqrt{2N}\cos\left((\omega_o + \omega_m)t + \phi(t)\right) \tag{10.22}$$

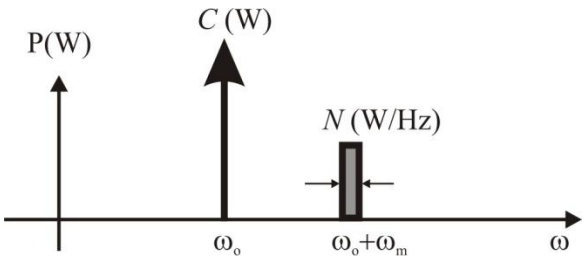


Figure 10.23 Center frequency component and noise

Expanding equation (10.22) using the additive theorem of trigonometric functions and assuming that $C >> N$, equation (10.23) below is obtained.

$$v(t) = \sqrt{2C}\cos\left(\omega_o t + \sqrt{\frac{N}{C}}\sin\left(\omega_m t + \phi(t)\right)\right) \tag{10.23}$$

Thus, the power of the carrier component does not change but is only phase-modulated by the noise signal. Since the maximum phase variation is $(N/C)^{½}$, then the peak phase jitter becomes$(N/C)^{½}$. This can be determined simply by representing the spectrum of Fig. 10.23 on a simple phasor diagram. The sine wave becomes the phasor rotated counter-clockwise and the noise vector is placed at the end of the sine wave vector which becomes a rotating phasor with angular velocity ω_m as shown in Fig. 10.24. Therefore, the maximum phase error is obtained as:

$$\overline{\phi^2}(t) = \frac{N}{C}\left[\text{rad}^2/\text{Hz}\right] \tag{10.24}$$

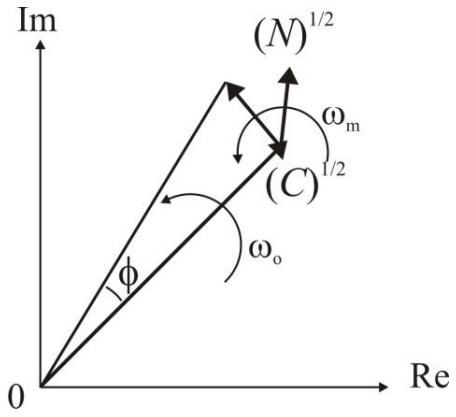


Figure 10.24 Phasor diagram

Thus, considering the spectrum example in Fig. 10.22, this phase fluctuation is a function of offset frequency and the phase jitter at the offset frequency of ω_m is

$$S_\phi(\omega_m) = \overline{\phi^2}(t) = \frac{N}{C} \tag{10.25}$$

■ Example 10.8

What is the peak phase jitter when the carrier to noise power at 100kHz offset is –100dB/Hz?

Solution

$$\frac{N}{C} = -100 \text{ dB/Hz},$$

Thus, the phase jitter=10^{-5} rad.

□■

10.3.3 Lesson's Phase Noise Model

The phase noise of an oscillator can be qualitatively explained in a simple model. In general, an oscillator can be represented as a circuit composed of an amplifier and a feedback network as shown in Fig. 10.25. Here, the frequency dependence of the amplifier gain is imposed on the feedback network, and the amplifier can be thought of as having a constant gain. In addition, the transfer characteristic of the feedback network can generally be expressed as in the following equation.

$$S_{21} = \frac{\beta_o}{1 + jQ\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)} \cong \frac{\beta_o}{1 + j2Q\left(\frac{\Delta\omega}{\omega_o}\right)} \tag{10.26}$$

where ω_o represents the oscillation frequency, $\Delta\omega=\omega-\omega_o=\omega_m$ represents the offset frequency. Generally, the magnitude of the frequency response in (10.26) is can be approximated constant while the phase can be seen to decrease linearly within the 3-dB bandwidth of $BW= \omega_o/Q$.

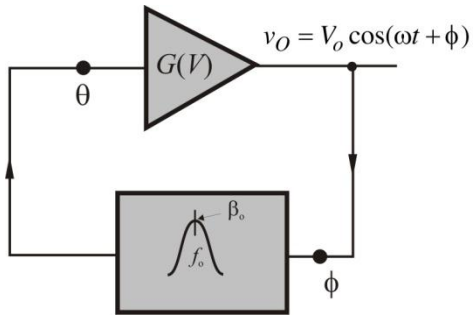


Figure 10.25 A simplified oscillator structure

The equivalent noise source in the oscillator circuit in Fig. 10.25 can be thought of appearing at the amplifier input, and its frequency characteristic is as shown in Fig. 10.26. *F* in Fig. 10.26 represents the noise figure. This noise will be added to the oscillator signal.

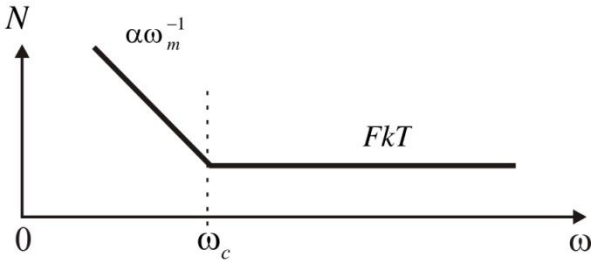


Figure 10.26 Noise at the amplifier input terminal

Assuming that the oscillation signal is frequency modulated by the noise signal as shown in Fig. 10.26 due to the nonlinearity of the amplifier, the frequency modulated signal then appears at the output of the amplifier. Denoting the peak frequency deviation of the frequency modulated signal by the noise as $\Delta\omega$, this is in turn is input to the feedback network, and appears at the input of the amplifier again. Also note that $\Delta\omega$ is function of offset frequency and is proportional to the noise characteristics shown in Figure 10.26.

When the output which is frequency modulated by the noise is applied to the input of the feedback network, the frequency modulated signal is transformed into a phase modulated signal by the feedback network. The peak phase deviation $\Delta\theta$ of the phase modulated signal is related the peak frequency deviation as

$$\Delta\theta = -\frac{2Q}{\omega_o}\Delta\omega \tag{10.27}$$

Thus, the phase-modulated signal given by equation (10.27) will appear at the input of the amplifier. Also note that, $\Delta\omega$ is proportional to the frequency characteristics of the noise shown in Fig.10.26 and $\Delta\theta$ is also proportional to the frequency characteristics of the noise in Fig.10.26. Since the phase noise represented by equation (10.25) corresponds to the peak phase deviation $\Delta\theta$, denoting the oscillator output power as *C*, the phase noise at the input terminal of the amplifier can be represented as shown in Fig. 10.27. Thus, the phase noise of the amplifier input can be written as

$$S_\theta(\omega_m) = \frac{FkT}{C}\left(1+\frac{f_c}{f_m}\right) \tag{10.28}$$

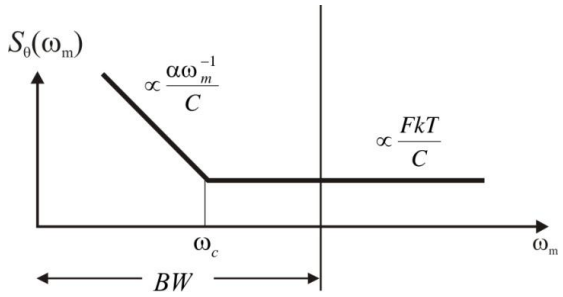


Figure 10.27 The phase noise at the amplifier input

Furthermore, the peak frequency deviation $\Delta\omega$ is related to the output peak phase deviation $\Delta\phi$ by $\Delta\omega=\omega_m\Delta\phi$. Thus, using equation (10.27), the relationship between the phase noise appearing at the amplifier input and the phase noise appearing at the oscillator output is obtained as

$$S_\theta(\omega_m)=\left(\frac{2Q\omega_m}{\omega_o}\right)^2 S_\phi(\omega_m) \tag{10.29}$$

In addition, outside the resonator bandwidth *BW*, there is no such relationship and is thus set follows:

$$S_\theta(\omega_m)=S_\phi(\omega_m) \tag{10.30}$$

Therefore, combining equations (10.29) and (10.30), the combined $S_\phi(\omega_m)$ can be written as

$$S_\phi(\omega_m)=S_\theta(\omega_m)\left[1+\left(\frac{\omega_o}{2Q\omega_m}\right)^2\right] \tag{10.31}$$

This is shown in Fig. 10.28.

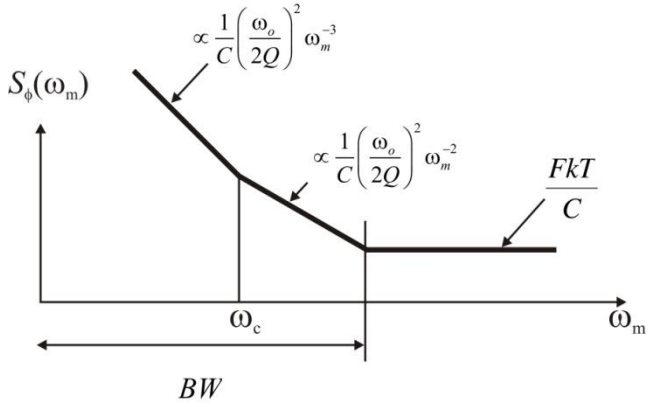


Figure 10.28 Phase noise Characteristics

That is, near the oscillation frequency, the phase noise decreases by ω^{-3} (30 dB / decade), and after the 1/*f* noise disappears, it decreases by ω^{-2} (20 dB / decade), and then outside the bandwidth of the resonator, it is proportional to the noise figure and shows a constant phase noise. Also noteworthy is that, the higher the *Q* of the feedback network, the lower the phase noise.

The Lesson model is based on deduction and must be proven in a number of ways. The assumption of frequency modulation by the noise at the amplifier input, namely the proportional relationship between the peak frequency deviation and the noise frequency characteristics was experimentally carried out by Pucel [9]. Pucel measured the 1/*f* noise of the drain current under a given DC voltage for a GaAs FET. The fluctuation of the drain current observed with a spectrum analyzer is shown in Fig. 10.29 (baseband noise in Fig. 10.29). Using this drain current fluctuation,

peak frequency deviation $\Delta\omega$ of the frequency modulated oscillation output can be calculated. This is usually referred to as FM noise. In this case, the frequency dependence of the FM noise must be the same as the drain current noise since this is a proportional relationship. The measured and computed FM noises as shown in Fig. 10.29 are found to have the same frequency characteristics of the drain current noise.

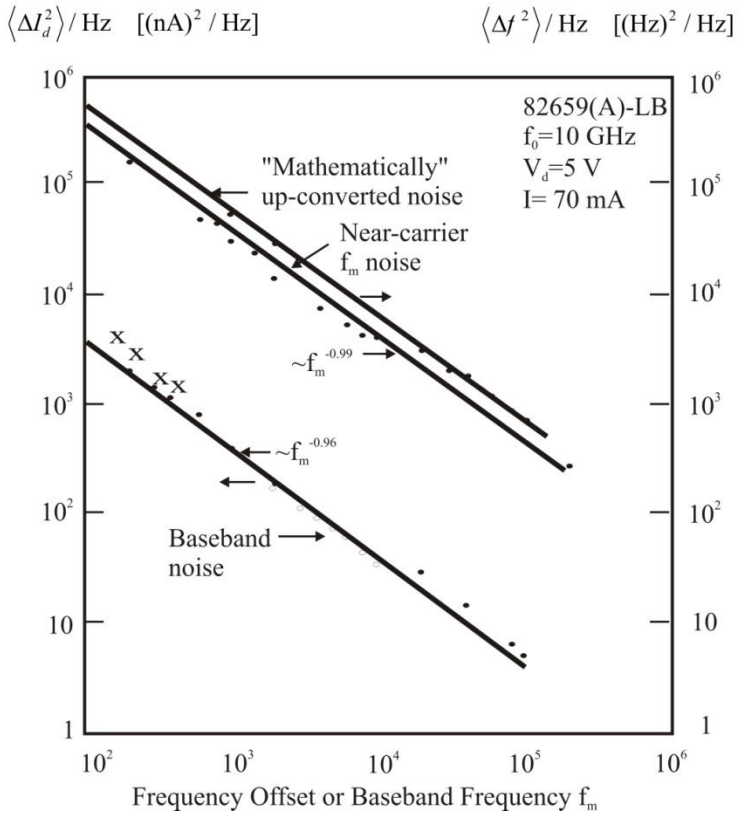


Figure 10.29 Pucel experimental results of oscillator phase noise [9]

10.3.4 Comparison of Oscillator Phase Noises

It is often necessary to compare the performance of oscillators in terms of phase noise even though the oscillators generally have different oscillation frequencies. To compare the phase noise of two oscillators with different oscillation frequencies, the frequencies of the oscillators must first be made equal by dividing or multiplying one of the frequencies. Firstly, we examine the changes in phase noise resulting from such frequency multiplication or division.

Given that the time-domain waveform of the oscillator is given by

$$v(t) = \sqrt{2C}\left(1 + a(t)\right)\cos\left(\omega_o t + \phi(t)\right) \tag{10.32}$$

Then after the frequency multiplication by n, the resulting output waveform can be expressed as:

$$v(t) = \sqrt{2C}\left(1 + a(t)\right)\cos\left(n\omega_o t + n\phi(t)\right) \tag{10.33}$$

Thus, the phase noise of the multiplied waveform is expressed as

$$S_{\phi}(\omega_m) = \overline{n^2\phi^2(t)} = n^2\overline{\phi^2}(t) \tag{10.34}$$

which represents a degradation of the phase noise by n^2. As an example, the change in phase noise of a 10 MHz crystal oscillator after multiplying its frequency to 10 GHz is shown in Fig.10.30. Since n = 1000, the phase noise can be seen to have increased by 60 dB in Fig. 10.30.

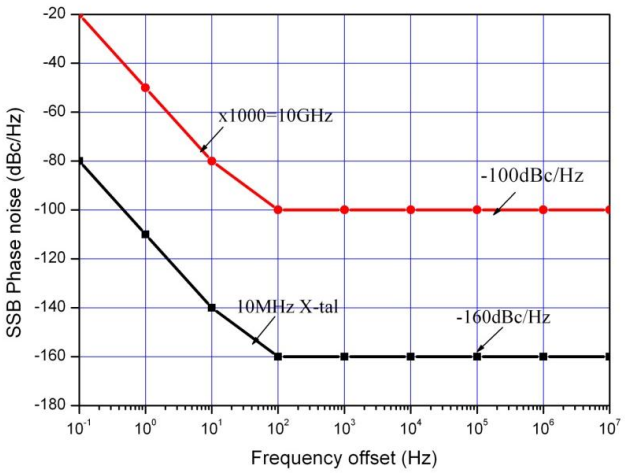


Figure 10.30 Comparison of oscillator phase noise when the frequency is multiplied by a factor.

In this way, the phase noises of various oscillators can be compared. Figure 10.31 shows the phase noises of various oscillators, *i.e.*, crystal oscillator, DRO (Dielectric Resonator Oscillator), and microstrip VCO (Voltage Controlled Oscillator). Their oscillation frequencies are: 10 MHz for crystal oscillator, 1 GHz for DRO and 10 GHz for the microstrip VCO. Thus, the performance of the oscillators can be compared by multiplying their oscillation frequencies to make all of them have a frequency of 10 GHz.

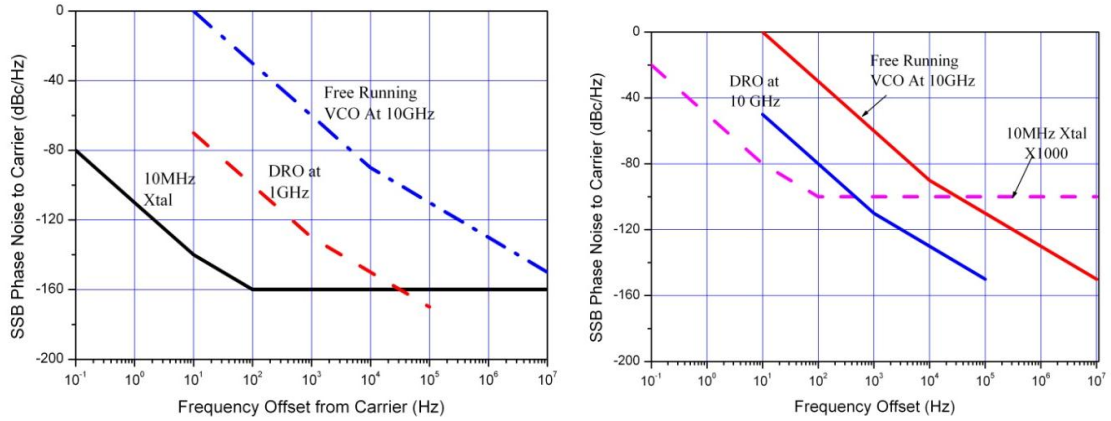


Figure 10.31 (a) Phase noise of various oscillators (b) and its multiplied phase noise

The phase noises of the oscillators after multiplying their frequencies to 10 GHz are shown in Fig. 10.32, and from this figure, the noise floor of the crystal oscillator (from the result of multiplying the frequency by a factor of 1000) has become higher, but compared to the other oscillators at low frequency, the phase noise can be seen to be low. This is followed by DRO, and the microstrip VCO can be seen to have the poorest phase noise.

■ Example 10.9

Compare the phase noise characteristics of a VCO having center frequency of 10 GHz and a phase noise of –100 dBc / Hz at 100 kHz frequency offset with another VCO having center frequency of 35 GHz and a phase noise of –96 dBc / Hz at 100 kHz frequency offset.

Solution
Assuming that the frequency of the 10 GHz VCO is to be multiplied to 35 GHz, then

$$n = \frac{35}{10}$$

The phase noise of the 10 GHz VCO after multiplying its frequency to 35 GHz equals

$$S_\phi = -100 + 10\log\left(\frac{35}{10}\right)^2 = -89 \text{ dBc/Hz}$$

Thus, the phase noise of the 10 GHz VCO can be seen to be poorer than that of the 35 GHz VCO by 7 dB.

□■

10.4 BASIC OSCILLATOR CIRCUITS

10.4.1 Canonical Oscillator Circuits

What was described earlier in Section 10.2.2 is related to the determination of the possibility of oscillation for a given oscillator circuit. However, designers should design oscillator circuits which oscillate at a certain desired frequency. This can be carried out using canonical oscillator circuits. Firstly, after removing the DC bias and DC decoupling circuits, and all the elements which have no effects at RF, most oscillator circuits can largely be categorized into two configurations. They can be classified into series feedback oscillators as shown in Fig. 10.32 (where *jy* is used in the series feedback to connect the output of the transistor DS to the GS input) or parallel feedback oscillators as shown in Fig. 10.33 (where *jy* is used in the parallel feedback to connect the DS output to the GS input). Three types of series feedback oscillator configuration are shown in Fig. 10.32, whereas Fig. 10.33 shows three types of parallel feedback oscillator configuration.

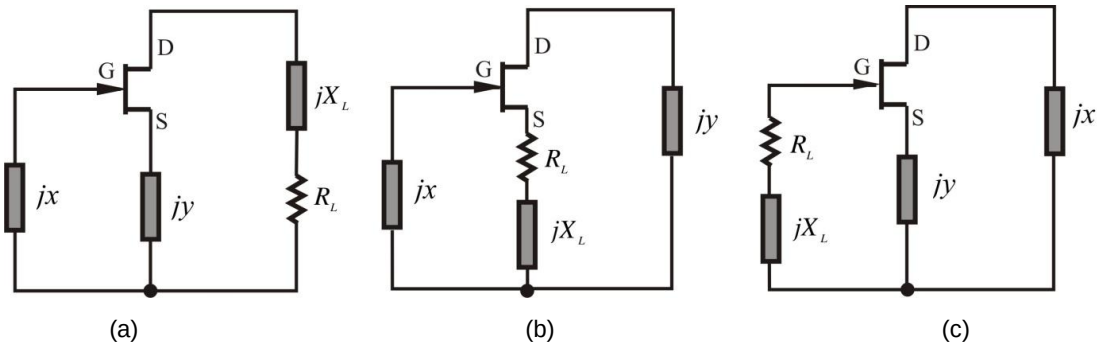


Figure 10.32 Three series feedback oscillators

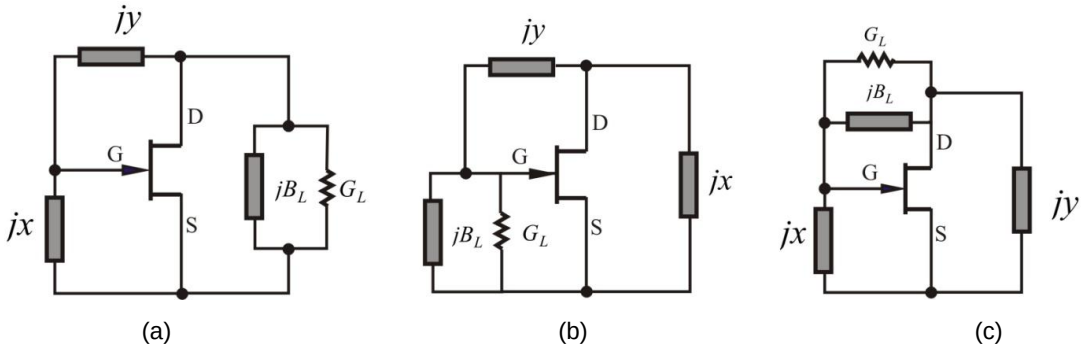


Figure 10.33 Three parallel feedback oscillators

The three forms of configuration in Fig. 10.32 and 10.33 are classified based on how the loads are connected; whereas the form of the feedback can be found to be essentially the same. In addition, *jx* and *jy* in the figure represent the reactance of a capacitor or inductor in the series feedback configurations, while they represent the susceptance of a capacitor or inductor in the parallel feedback configurations.

Such basic forms of oscillator circuit can be represented by an amplifier and a feedback network. The basic form of the series oscillator in Fig. 10.32 can be converted into the T-type feedback network in Fig. 10.34(a), and the basic form of the parallel feedback oscillator can be converted into Pi-type feedback network in Fig.10.34(b).

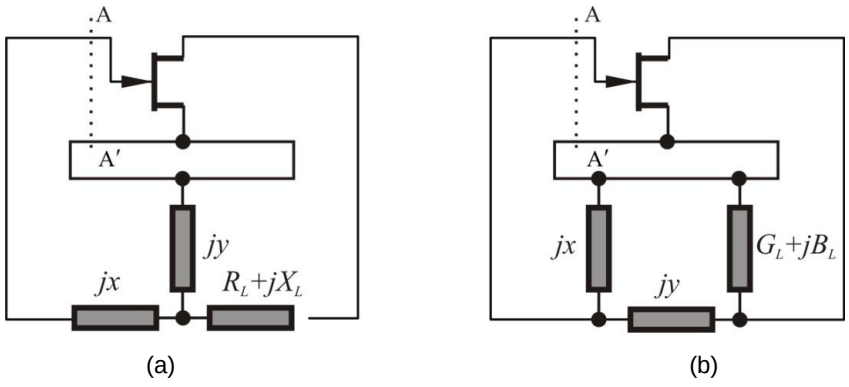


Figure 10.34 (a) T-type feedback network and (b) Pi-type feedback network

The mechanism of oscillation of such series or parallel configuration can be qualitatively known by analyzing the feedback structure. First, for the series configuration of Fig. 10.32(a), the reactance *jx* can be represented by capacitor, the reactance *jy* of the feedback network by inductor and the load by a capacitor and resistor in series as shown in Fig. 10.35. In addition, since the input impedance of the transistor at high frequencies is typically low, approximating it as short, the open loop circuit can essentially be represented by the equivalent circuit of Fig. 10.36 in which the DS output voltage of the transistor varies in proportion to the input current. To obtain the open-loop gain, the A–A' reference plane in Fig. 10.34 is broken and a unit current source is applied to the transistor input. As the input impedance of the transistor is approximated as short, a shorted load can be connected where the cut occurs. This is shown in Fig. 10.36. The open-loop gain is then $-I_r$ of Fig. 10.36.

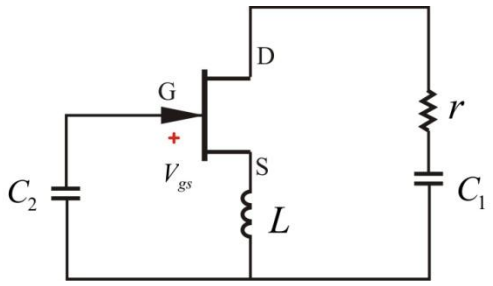


Figure 10.35 Implementation example of Figure 10.33(a)

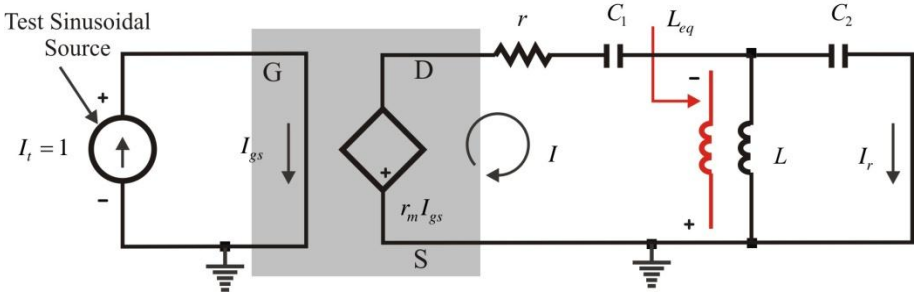


Figure 10.36 Open loop circuit of the circuit in Fig. 10. 34(b)

Here, the parallel impedance of L, C_2 is

$$j\omega L_{eq} = \frac{j\omega L \bullet \dfrac{1}{j\omega C}}{j\omega L + \dfrac{1}{j\omega C}} = \frac{j\omega L}{1-\omega^2 LC_2} = \frac{j\omega L}{1-\dfrac{\omega^2}{\omega_r^2}} \tag{10.35a}$$

$$\omega_r^2 = \frac{1}{LC_2} \tag{10.35b}$$

Thus, at frequencies lower than ω_r, L and C_2 connected in parallel are equivalently treated as an inductor of value L_{eq}. In addition, since the current transfer function I_r/I becomes

$$k = \frac{I_r}{I} = \frac{j\omega L}{j\omega L + \dfrac{1}{j\omega C_2}} = \frac{1}{\left(1 - \dfrac{\omega_r^2}{\omega^2}\right)}, \tag{10.36}$$

At frequencies lower than ω_r, the phase of k becomes 180° and a phase inversion occurs. In contrast, at frequencies higher than ω_r, the phase becomes 0° and resulting in the disappearance of the phase inversion. It also is worth noting that k is a real number. Furthermore, the open-loop gain becomes

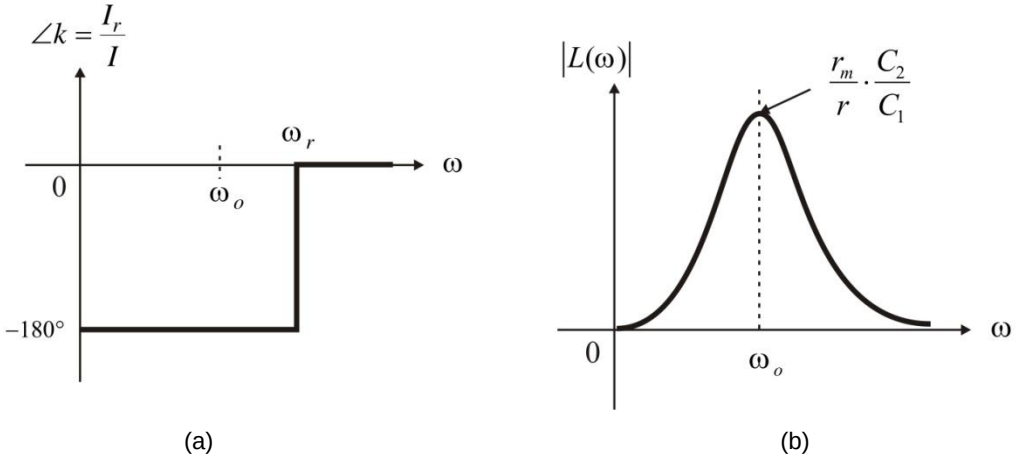
$$L = -k \cdot \frac{r_m}{r + \dfrac{1}{j\omega C_1} + j\omega L_{eq}} = -k \cdot \frac{r_m}{r + \dfrac{1}{j\omega C_1}\left(1 - \dfrac{\omega^2}{\omega_o^2}\right)} \tag{10.37a}$$

$$\omega_o^2 = \frac{1}{L\left(C_1 + C_2\right)} \tag{10.37b}$$

Since $\omega_o < \omega_r$ at $\omega = \omega_o$ where the open-loop gain is real, the result of equation (10.37a) is a positive real number and therefore the phase of the open-loop gain can be seen to be 0. The open-loop gain then is

$$L\left(\omega_o\right) = \frac{C_2}{C_1}\frac{r_m}{r} \tag{10.38}$$

When this gain is greater than 1, it is evident that oscillation will occur. Thus, phase inversion occurs due to $L_2 \| C_2$ and the oscillation frequency occurs at the resonant frequency of $L_2 \| (C_1 + C_2)$, and when the gain given by equation (10.38) is greater than 1, oscillation can be seen to be formed. This is shown in Fig. 10.37.



(a) (b)

Figure 10.37 (a) Current transfer characteristics and (b) open-loop gain characteristics

In the case of parallel feedback oscillator in Fig. 10.33(a), the circuit can be represented as shown in Fig. 10.38 by replacing the reactance *jx* with a capacitor, the feedback reactance *jy* with an inductor and the load with a capacitor and resistor in parallel. Furthermore, the input impedance of the transistor at low frequencies is generally high; the transistor can be approximately represented by an equivalent circuit where the input is open, and the drain current varying according to the input voltage. Similar to the previously discussed series feedback type oscillator, to obtain the open-loop gain, the circuit is cut at the cutting plane of Fig. 10.34(b) and the transistor is replaced by the equivalent circuit leading to the equivalent circuit of Fig.10.39. As shown in the figure, a unit voltage source is applied to the input, and the open-loop gain is obtained by calculating the voltage V_r returning from the output to the input.

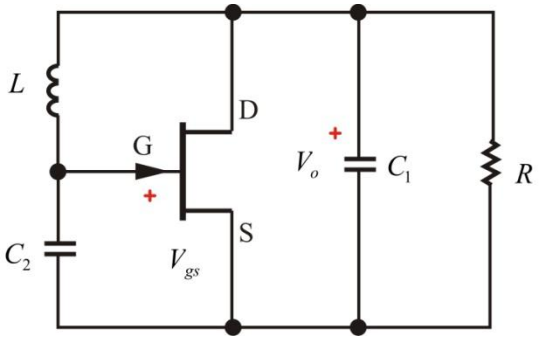


Figure 10.38 Example of parallel feedback oscillator circuit

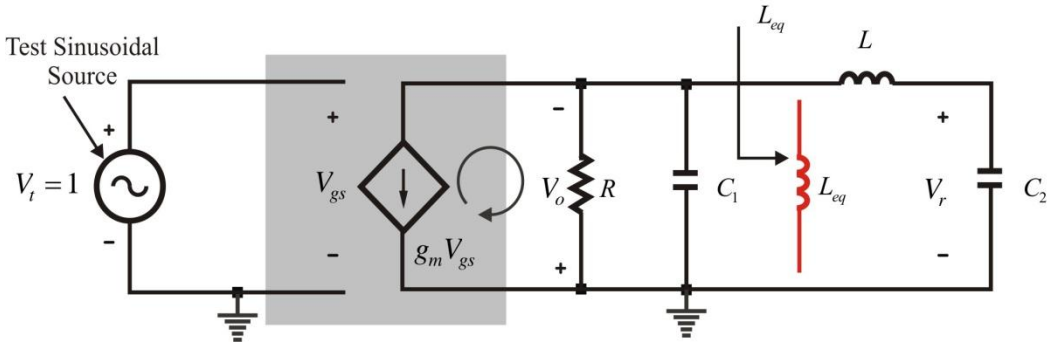


Figure 10.39 Equivalent circuit of a parallel oscillator circuit

From the figure, the voltage transfer function computed as $k=V_r/V_o$ is given by

$$k = \frac{\dfrac{1}{j\omega C_2}}{\dfrac{1}{j\omega C_2} + j\omega L} = \frac{1}{1-\dfrac{\omega^2}{\omega_r^2}} \tag{10.39a}$$

$$\omega_r^2 = \frac{1}{LC_2} \tag{10.39b}$$

Thus, phase inversion appears for frequencies higher than ω_r and disappears for frequencies lower than ω_r. In addition, as in the case of series feedback, k is a real number. Furthermore, the open-loop gain is

$$L = V_r = -g_m \frac{Z_t R}{R + Z_t} k \tag{10.40a}$$

$$Z_t = \frac{\frac{1}{j\omega C_1}\left(\frac{1}{j\omega C_2} + j\omega L\right)}{\frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} + j\omega L} \tag{10.40b}$$

Thus, the open-loop gain is:

$$L = V_r = -g_m \frac{1}{j\omega\left(C_1 + C_2\right)\left(1 - \omega^2 L C_1 \| C_2\right) + G\left(1 - \omega^2 L C_2\right)} \tag{10.41}$$

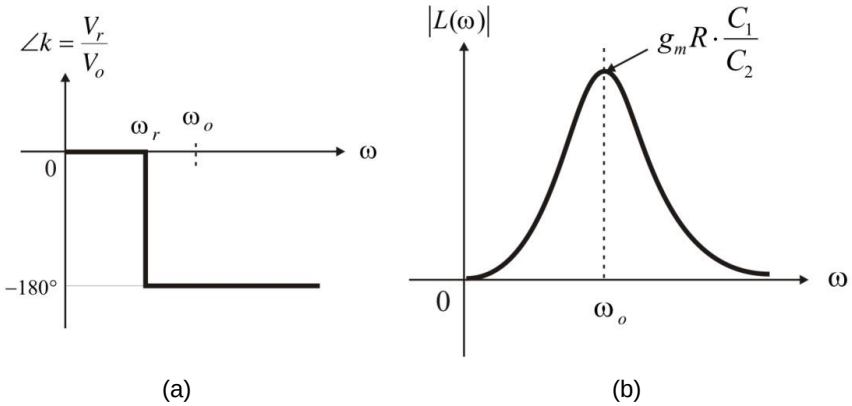
Since the imaginary part of the denominator of the above expression must be 0, for oscillation to occur, the oscillation frequency

$$\omega_o^2 = \frac{1}{L(C_1 \| C_2)} \tag{10.42}$$

It can also be seen that $\omega_o > \omega_r$. Then, substituting this into the gain equation, the following condition must be satisfied for oscillation to occur.

$$L\left(\omega_o\right) = -g_m \frac{1}{1 - \frac{1}{LC_1 \| C_2} LC_2} = g_m R \frac{C_1}{C_2} > 1 \tag{10.43}$$

Thus, no oscillation occurs when the open-loop gain given by equation (10-43) is less than 1. From equation (10.42), it can be found that the oscillation frequency is the resonant frequency of the overall LC resonant circuit seen from the output. Furthermore, since $\omega_o > \omega_r$, the value of k can be seen to be negative. That is, the oscillation frequency must always be higher than this frequency that causes the phase inversion. Because the amplifier is an inverting amplifier which has its own phase inversion of 180°, the k network should provide the phase inversion of 180° to restore the overall phase of the open loop gain to 0°. This is shown in Fig. 10.40.



(a) (b)

Figure 10.40 (a) Voltage transfer characteristics and (b) Open-loop gain characteristics

10.4.2 Conversion to Basic Forms

The series and parallel basic forms described above represent equivalent circuits at RF frequency and the actual oscillator circuit is realized by applying DC voltage to the former and which is also modified to deliver the appropriate part of oscillation output power to the load. The resulting circuit looks slightly different from the basic forms. However, these oscillators when simplified can mostly be converted to the previously mentioned basic forms of the oscillator. Thus, for a given oscillator circuit, the design tasks involve firstly, the conversion of the oscillator circuit to one of the basic forms and secondly application of DC voltage to a selected basic form of oscillator circuit. In this section, we will study more about these tasks through some examples.

■ Example 10.10

The following is a microstrip oscillator circuit. Simplify this circuit and determine which form of the basic oscillator circuit it is.

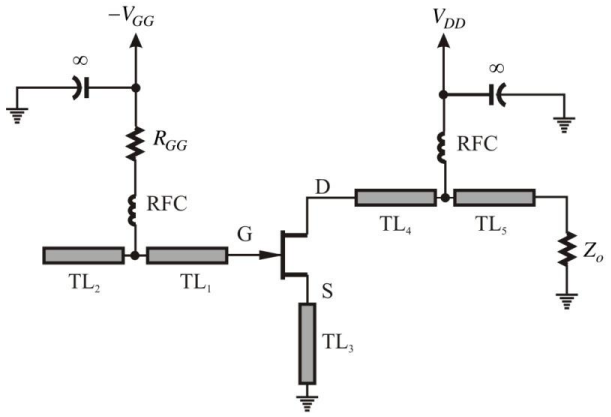


Figure 10E.16 Microstrip oscillator circuit

Solution

Removing the DC bias circuit portion of Fig. 10E.16 results in the bottom-right circuit diagram in Fig. 10E.17.

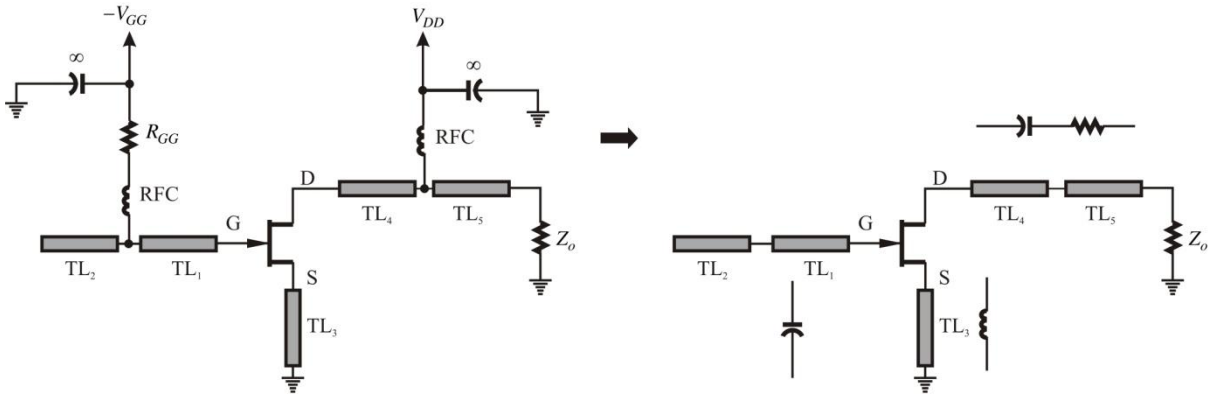


Figure 10E.17 Simplified oscillator circuit

The circuit connected to the drain terminal can be seen as RC series circuit at the oscillation frequency, and also assuming the length of transmission line is short, then the transmission line connected to the source can be seen as an inductor. Furthermore, the two transmission lines connected to the gate terminal can be considered as capacitor, and by removing ground, this circuit can be equivalently re-drawn as the basic form of the series feedback oscillator in Fig. 10.35.

■

■ Example 10.11

The following circuit in Fig. 10E.18 is a 200 MHz band Colpitts oscillator [1]. Convert this into a parallel feedback basic type and calculate the values of the resulting feedback admittance *jx*, *jy*, and the load admittance $G_L + jB_L$ at 200 MHz using ADS.

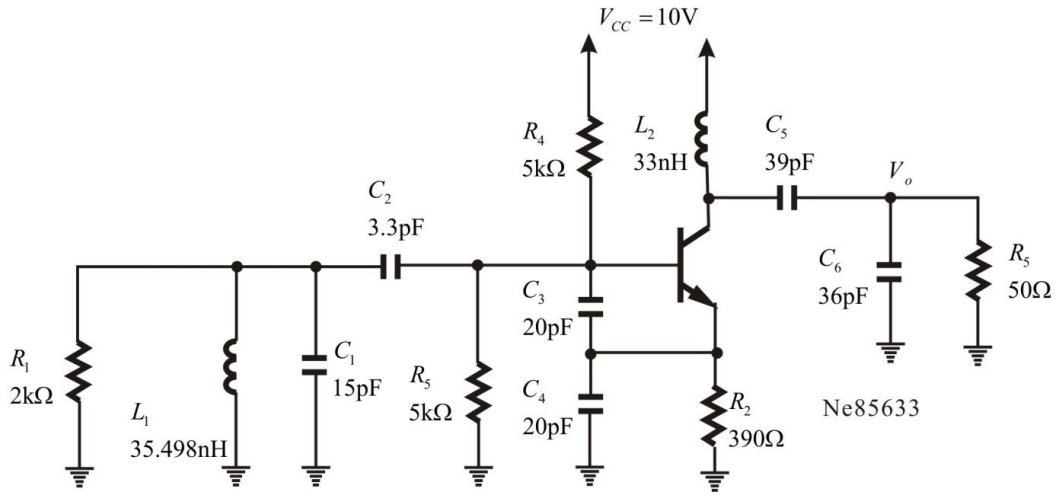


Figure 10E.18 A 200 MHz Colpitts oscillator circuit

Solution

After removing the ground point in Fig. 10E.18, and moving the new ground to the emitter of the transistor, the two-port parameter values of the feedback network to the transistor can be obtained by removing the transistor as shown in Fig. 10E19. This is shown in Fig. 10E.19.

The Y-parameters of the 2-port circuit thus defined as in Fig. 10E.19 can now be obtained, which can be represented by the Pi-type circuit shown in Fig. 10.34(b). Since it is a passive network, $y_{11}+y_{12}$ correspond to the admittance *jx* of the basic form of the parallel feedback oscillator and $y_{22}+y_{12}$ corresponds to $Y_L=G_L+jB_L$ while *jy* corresponds to $-y_{12}$. Therefore, the following equations are inserted in the Display window and the values of the admittances are displayed using **listing**.

```
Eqn jx=Y(1,1)+Y(1,2)
Eqn jy=-Y(1,2)
Eqn YL=Y(2,2)+Y(1,2)
```

jx	*jy*	Y_L
$1.8541\times10^{-2}+j2.9972\times10^{-2}$	$1.7236\times10^{-3}-j3.5450\times10^{-3}$	$2.4685\times10^{-3}+j4.3726\times10^{-3}$

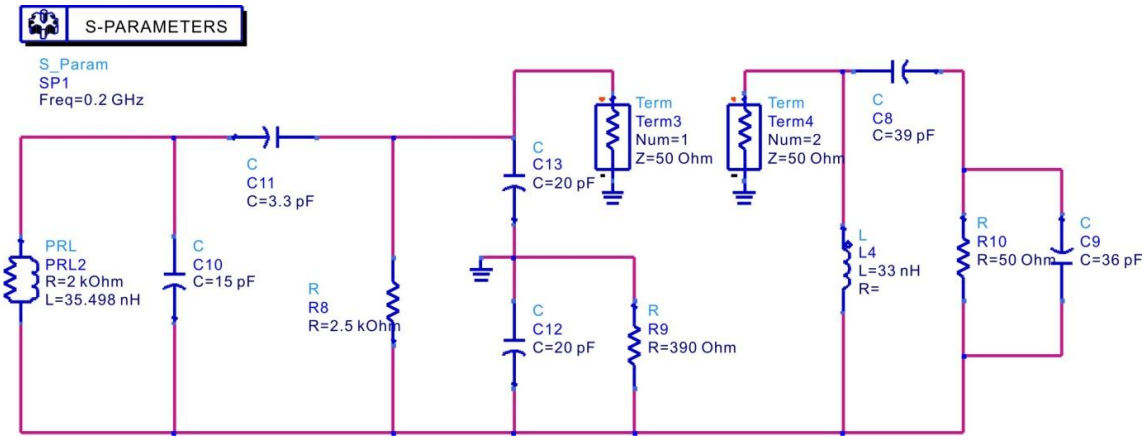


Figure 10E.19 Calculation of the two-port circuit parameters external to the oscillator

Here, *jy* is an inductor, Y_L and *jx* can be seen to be capacitors. However, it can be seen that, *jx* and *jy* are not pure imaginary numbers, which is because; the collector terminal of the transistor in Fig. 10E.18 is not connected to ground but to a 33 nH inductor. Next, in order to confirm the open-loop gain at 200MHz, the S-parameter of NE85633 is inserted and simulated in ADS as shown Fig. 10E.20.

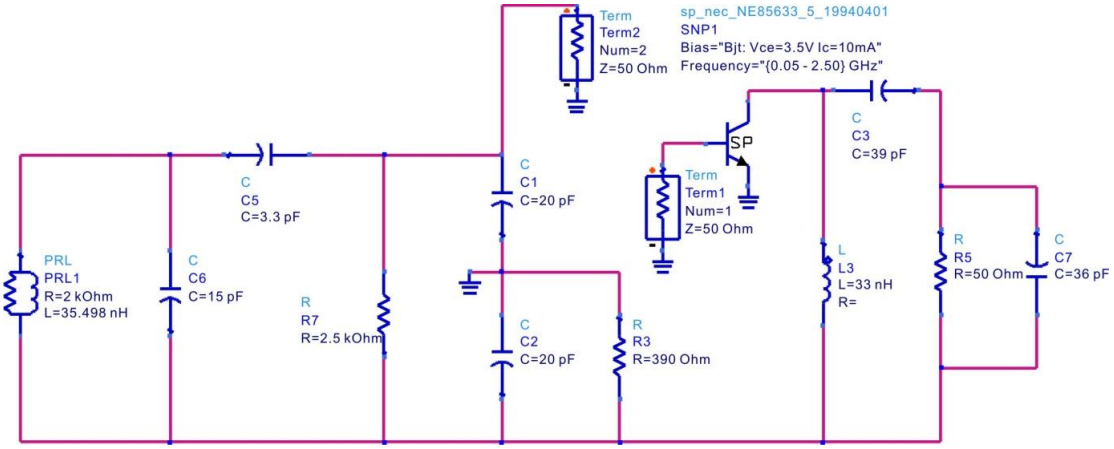


Figure 10E.20 Circuit for calculation of the open loop gain

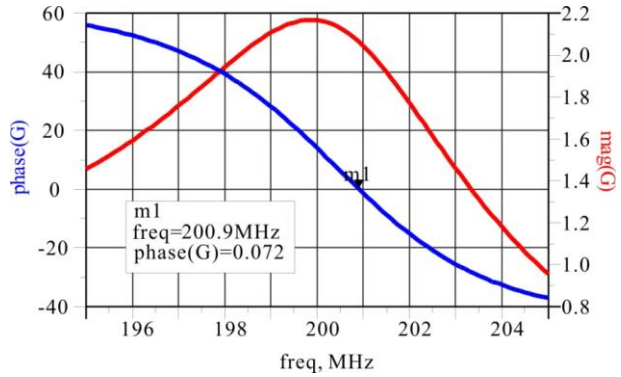


Figure 10E.21 Open-loop gain calculation result

The calculated open-loop gain is shown in Fig. 10E.21 and the oscillation condition can be seen to be satisfied at a frequency of approximately 200.9 MHz.

□■

■ Example 10.12

Replace the FET in the basic parallel type oscillator in Fig. 10.38 with a BJT, and put the ground point at the collector, and then implement the oscillator circuit by adding DC bias.

Solution

The circuit in the case of a common collector is as shown in Fig. 10E.22. The collector DC voltage is supplied through the bypass capacitor, and the oscillation output is obtained from the emitter terminal. In addition, the DC voltage to the base is supplied using bias resistors R_1 and R_2. Furthermore, a DC block capacitor is inserted between the inductor and base to prevent the base from being grounded. The emitter current of the BJT can then be set by the resistor R_E. Also, DC block capacitor is required to prevent the appearance of DC voltage at the output. The inserted resistors, whose impedances at the oscillation frequency should be higher than those of the components around them, must be set so as not to affect the RF signal at oscillation frequency. The common collector implementation is easy and thus widely used. The Colpitts oscillator circuits of Fig. 10E.13 and Fig. 10E.18 can be considered as a variant of the implementation of the common-collector oscillator circuit. In particular, in order to reduce the impact of the emitter bias resistor, RFC may be used as shown in Fig. 10E.13. It must be noted that, because the DC block capacitors and RFCs inserted for DC bias can be possibly made to satisfy the oscillation conditions at other undesired frequencies, the appropriate values of DC block capacitors and RFCs which do not satisfy these oscillation conditions should be chosen. Besides, rather than the collector as the ground, the ground can be set as the emitter or the base. However, these kinds of configuration are not widely used due to the complexity of their implementations.

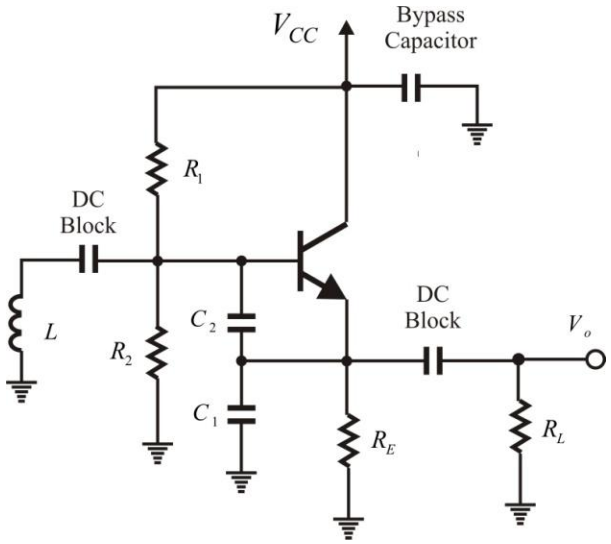


Figure 10E.22 Implemented Colpitts oscillator

□■

10.4.3 Design Method

Oscillator design from the impedance point of view is relatively simple. That is, the reference plane is set at the active part which could be Gunn or IMPATT diodes, and a series resonant load at the oscillation frequency is formed by adding a matching circuit to the 50 ohm load. The matching circuit must be designed such that, the resistance looking into the load from the active part is smaller than the negative resistance of the active part. Alternatively, from the admittance point of view, a parallel resonant load is formed by adding a matching circuit to the 50 ohm load and the matching circuit must be designed such that, the value of the parallel load is greater than the negative resistance of the active part.

This concept can similarly be applied to the design of series or parallel feedback type oscillators. In the case of the series feedback type, the reference plane is set at the terminating reactance jx as shown in Fig. 10.41(a) and the active part is designed to satisfy the oscillation condition. For the purpose of a simple design, the load $Z_L=R_L+jX_L$ is set as $X_L=0$, $Z_L=Z_o$ and the series feedback reactance jy giving the appropriate negative resistance value can be found by varying jy. Now, denoting the impedance looking into the active part from the reference plane as Z_{in}, the oscillation condition can be satisfied by setting the value of jx as $x= -\text{Im}(Z_{in})$. Next adding the DC bias circuits for the transistor completes the oscillator design. This design method is simple; however, when the gain of the transistor is not high, the negative resistance is not induced at the reference plane which causes problems in oscillator design. In that case, the design can be accomplished by adjusting the value of the load impedance Z_L through trial and error.

Alternatively, the reference plane is set at the load as shown in Fig. 10.41(b) and the reactance pair jx and jy are set to make the real part of the impedance Z_{in} seen from the load Z_L negative. The selection of these reactive pair is possible when the contour of the real part of Z_{in} is plotted in the (x, y) plane. The method of plotting such contours can be found in Appendix D, and by using such method, the (x, y) values giving negative resistance can be selected. Thus, for the selected (x, y) values, the impedance Z_{in} seen from the load Z_L can be calculated. The suitable load Z_L for this Z_{in} can then be synthesized using a matching network to satisfy the oscillation conditions. The real part of the load Z_L must be less than the negative resistance of the set Z_{in}, and also Z_L+Z_{in} must be designed to be series resonant at the oscillation frequency. The basic form of the parallel oscillator can be designed using the admittance condition and a method similar to the design of the basic form of the series oscillator.

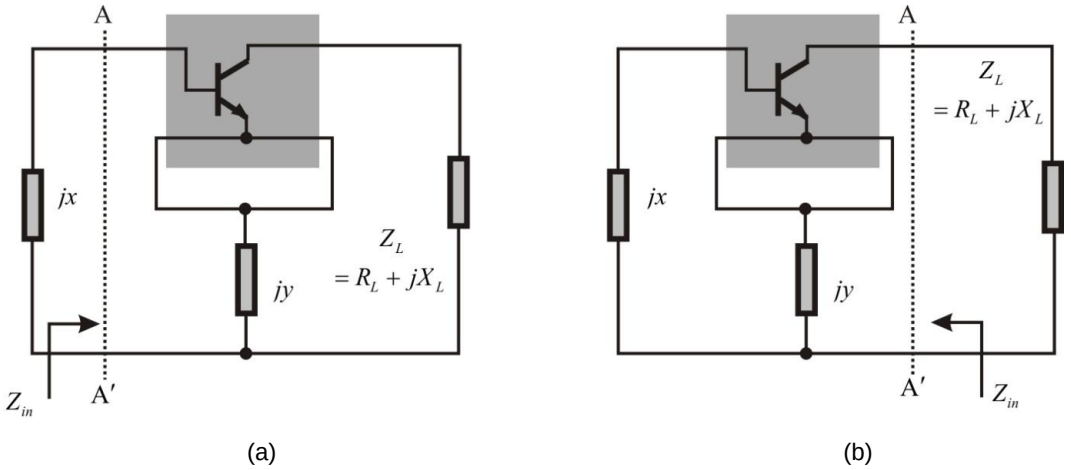


Figure 10.41 Design of feedback type oscillators: (a) jx reference plane and (b) load reference plane

The oscillation frequency for these one-port based oscillator designs can easily be determined, but that alone is not enough when this design method is applied to two-port devices such as a transistor. For example, one will not be able to know whether the transistor in the oscillator is set to give maximum gain or is set to give maximum output power. The 2-port method even though is more complex than the 1-port method can provide an improved design. Firstly, consider the transistor in Fig. 10.42 as an amplifier. For an input voltage V_1, once the load is known, the input current I_1 and output voltage and current I_2 and V_2 can also be determined. The load can be set by setting the transistor for maximum gain as well as for maximum output power by performing load-pull simulation. This is the same as the setting of the load impedance for maximum power gain or for maximum output power previously described in amplifier designs in Chapters 8 and 9.

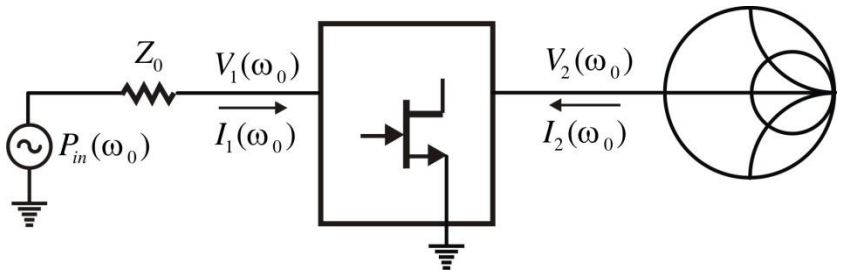


Figure 10.42 Determination of the input and output voltages and currents

Denoting the voltage and current thus obtained as V_1, V_2, I_1, and I_2 respectively, the feedback network should be designed to give such input and output voltages shown in Fig. 10.43. With these voltages and currents, the input power and oscillation output power are:

$$P_{in} = \mathrm{Re}\left(V_1^* I_1\right) \tag{10.44a}$$

$$P_L = -\mathrm{Re}\left(V_1^* I_1 - V_2^* I_2\right) \tag{10.44b}$$

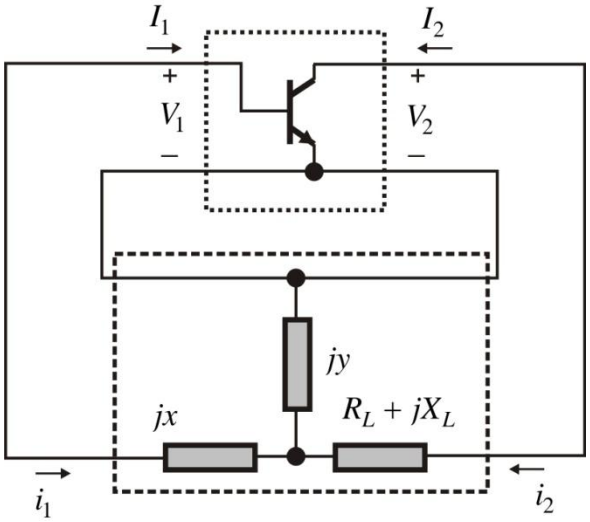


Figure 10.43 Definition of the voltages and currents in the oscillator

Furthermore, defining $i_1 = -I_1$, $i_2 = -I_2$ as shown in the figure, and denoting the Z-parameters of the external feedback network as Z^e, the terminal voltages V_1, V_2 can be expressed as

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} Z_{11}^e & Z_{12}^e \\ Z_{12}^e & Z_{22}^e \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \tag{10.45}$$

What needs to be determined is Z^e, as V_1, V_2 i_1, and i_2 have already been determined. The Z-parameters Z^e for the T-type circuit are:

$$Z_{12}^e = jy \tag{10.46a}$$

$$Z_{11}^e = jx + jy \tag{10.46b}$$

$$Z_{22}^e = Z_L + jy \tag{10.46c}$$

Thus, considering the real and imaginary parts, Z^e has four unknowns. In addition, considering the real and imaginary parts of equation (10.45) as independent, Z^e can completely be determined from the four equations. Defining new parameters as

$$z_1 = -V_1 / I_1 \tag{10.47a}$$

$$\beta_f = \left(1 + I_2 / I_1\right) \tag{10.47b}$$

$$z_2 = -V_2 / I_2 \tag{10.47c}$$

$$\beta_b = \left(1 + I_2 / I_1\right) \tag{10.47d}$$

The Z^e value giving the set V_1, V_2 I_1, and I_2 can be determined as follows:

$$Z_L = z_2 + j\beta_b \frac{\mathrm{Re}\left(z_1\right)}{\mathrm{Im}\left(\beta_f\right)} \tag{10.48a}$$

$$y = -j \frac{\mathrm{Re}\left(z_1\right)}{\mathrm{Im}\left(\beta_f\right)} \tag{10.48b}$$

$$jx = j\,\mathrm{Im}\left(z_1\right) + j\,\mathrm{Re}\left(\beta_f\right) \frac{\mathrm{Re}\left(z_1\right)}{\mathrm{Im}\left(\beta_f\right)} \tag{10.48c}$$

The settings of equation (10.48) makes the open loop gain for the set V_1, V_2, I_1, and I_2 equal to 1. In the case when the voltages and currents, V_1, V_2 I_1, and I_2 are not determined at the maximum output

power or large signal, a problem arises when the open loop gain equals to 1. That is, because generally, the gain at maximum output power is lower than the small-signal gain, even when the open-loop gain is 1, the small signal open-loop gain naturally becomes greater than 1 and does not cause major problems. However, because this setting corresponds to the threshold value in the case of small-signal, no oscillation can occur. Thus, the gain margin of the active device could be selected. Considering the output which is *back-off* by an amount equal to the power gain, g, V_2, and I_2 should each be back-off by an amount equal to $1/(g)^{½}$. That is,

$$V_2' = \frac{V_2}{\sqrt{g}}, \qquad I_2' = \frac{I_2}{\sqrt{g}} \tag{10.49}$$

The values for the feedback network can then be determined by substituting V_2' and I_2' into equations (10.47) and (10.48).

■ Example 10.13

Using NE42484 S-parameters at V_{DS}=2 V, I_{DS}=10 mA in ADS, set the power gain back-off value to g = 2 for a 50 ohm load at the frequency of 9.2 GHz, and determine the values of the series feedback network. Also plot the open-loop gain.

Solution

After entering the NE42484 S-parameters, the following schematic is set up to calculate the voltage and current for the 50 ohm load.

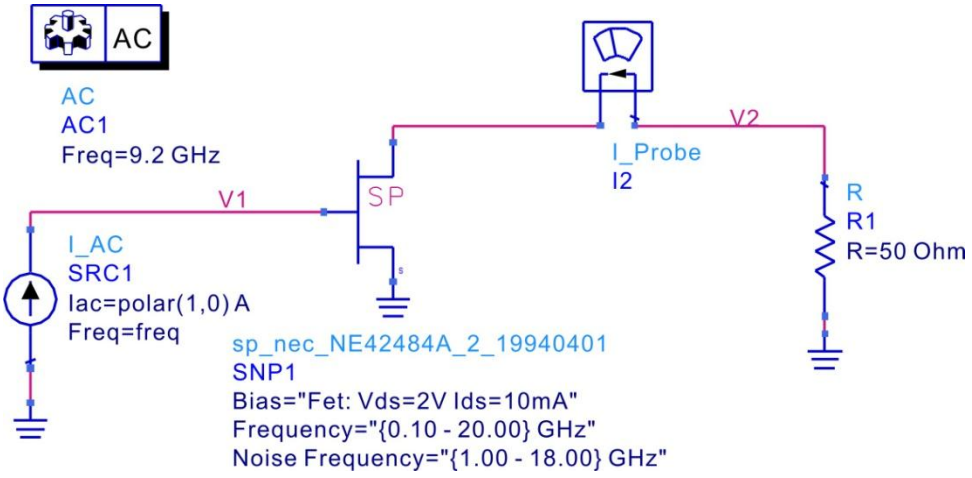


Figure 10E.23 Schematic to determine the current and voltage for the feedback network

After simulation, the following equations are inserted in the Display windows to obtain the parameters defined by equations (10.47).

Eqn g=2
Eqn z1=-V1
Eqn z2=-V2/I2.i

Eqn beta_f=1+I2.i/sqrt(g)
Eqn beta_b=1+1/(I2.i/sqrt(g))

Thus, the following equations are again inserted in the Display window to determine the value of the feedback network from the parameters defined in equation (10.48).

Eqn ZL=z2+j*beta_b*real(z1)/imag(beta_f)
Eqn y=-real(z1)/imag(beta_f)
Eqn x=imag(z1)+real(beta_f)*real(z1)/imag(beta_f)

The computed values are as shown in the table below.

x	y	ZL
16.317	-20.405	42.790 + j7.264

The circuit in Fig. 10E.24 for obtaining the open loop gain is configured to confirm whether the values in the above table give the desired open-loop gain.

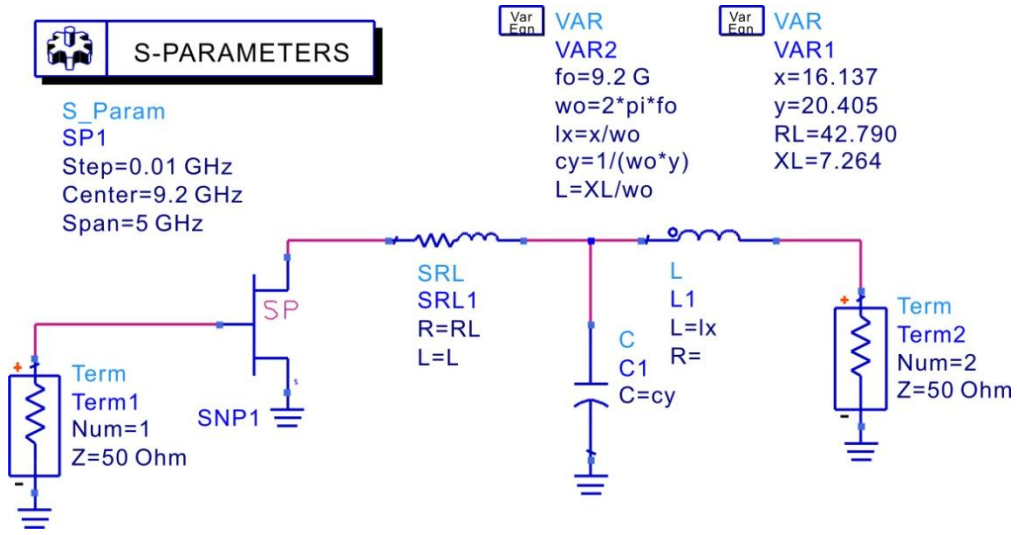


Figure 10E.24 Schematic for computing the open-loop gain

To calculate the open-loop gain from the S-parameter results, the following equation is inserted in the Display window to plot the open-loop gain.

Eqn G=(S(2,1)-S(1,2))/(1-S(1,1)*S(2,2)+S(1,2)*S(2,1)-2*S(1,2))

The open loop gain is as shown in Fig. 10E.25. From Fig. 10E.25, as expected, at the frequency of 9.2GHz where the phase is 0.138° which is close to 0, the open-loop gain is 1.408. Therefore, calculating the power gain,

$$10\log\left(1.408^2\right) = 2.97 \text{ dB},$$

which is close to the set value of the gain.

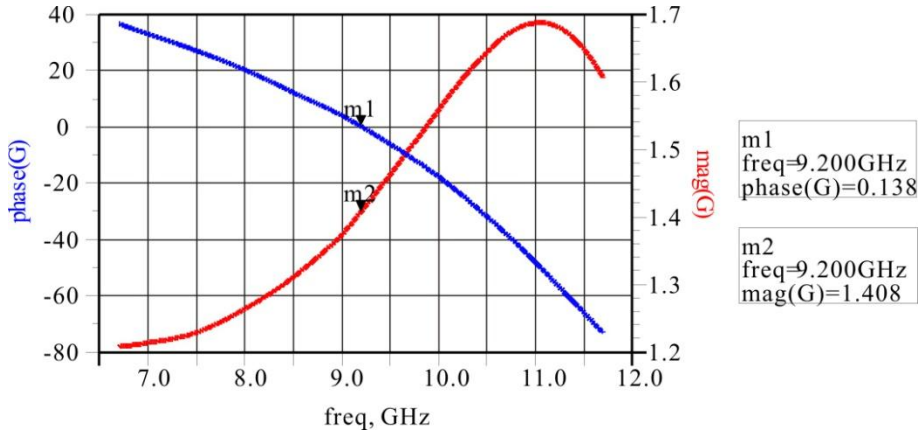


Figure 10E.25 Open-loop gain calculation results

■

In the case of Pi-type feedback network, similarly, defining the Y-parameters as Y^e and following a similar process, the following parameters can be defined for the Pi-type feedback network:

$$y_1 = -I_1/V_1 \tag{10.50a}$$

$$\beta_f = \left(1 - V_2/V_1\right) \tag{10.50b}$$

$$y_2 = -I_2/V_2 \tag{10.50c}$$

$$\beta_b = \left(1 - V_1/V_2\right) \tag{10.50d}$$

From these equations, the values for the feedback network can be determined as follows:

$$Y_L = y_2 + j\beta_b \frac{\mathrm{Re}\left(y_1\right)}{\mathrm{Im}\left(\beta_f\right)} \tag{10.51a}$$

$$jy = -j\frac{\mathrm{Re}\left(y_1\right)}{\mathrm{Im}\left(\beta_f\right)} \tag{10.51b}$$

$$jx = j\,\mathrm{Im}\left(y_1\right) + j\,\mathrm{Re}\left(\beta_f\right)\frac{\mathrm{Re}\left(y_1\right)}{\mathrm{Im}\left(\beta_f\right)} \tag{10.51c}$$

Generally, instead of the lossless *jx* and *jy* the case of lossy values of the feedback network can also be considered. In such a case, the feedback network values can be determined through a similar method by assuming fixed loss.

10.5 OSCILLATOR DESIGN EXAMPLES

10.5.1 Design of VCO for Mobile Communication

Figure 10.44 shows the configuration of a voltage-controlled oscillator (VCO) used for mobile communication. The voltage-controlled oscillator shown in Fig. 10.44 has a size of 12 × 10 × 4 mm, and a volume of approximately 4.8 cc. Presently, the VCOs are fabricated using the same technology but with even smaller sizes. As can be seen in Fig. 10.44, this VCO is composed of a metallic cover and a multilayer printed circuit board which is used to mount chip components for VCO. The metallic cover provides electromagnetic shielding and ground. Therefore, the total weight of the VCO is determined by the multilayer printed circuit board and the thin metal cover, which makes it a lightweight. Furthermore, the terminals for DC power supply, oscillator output, ground, and frequency tuning for VCO are formed by cutting the center of the through-hole of the multilayer printed circuit board into half, which results in the half-plated cylindrical shape terminals. Solder resist material is coated everywhere on the bottom of the printed circuit board except on the terminals for connection. This provides electrical isolation with the possible lines of PCB passing through the bottom of the VCO when the VCO is mounted on PCB.

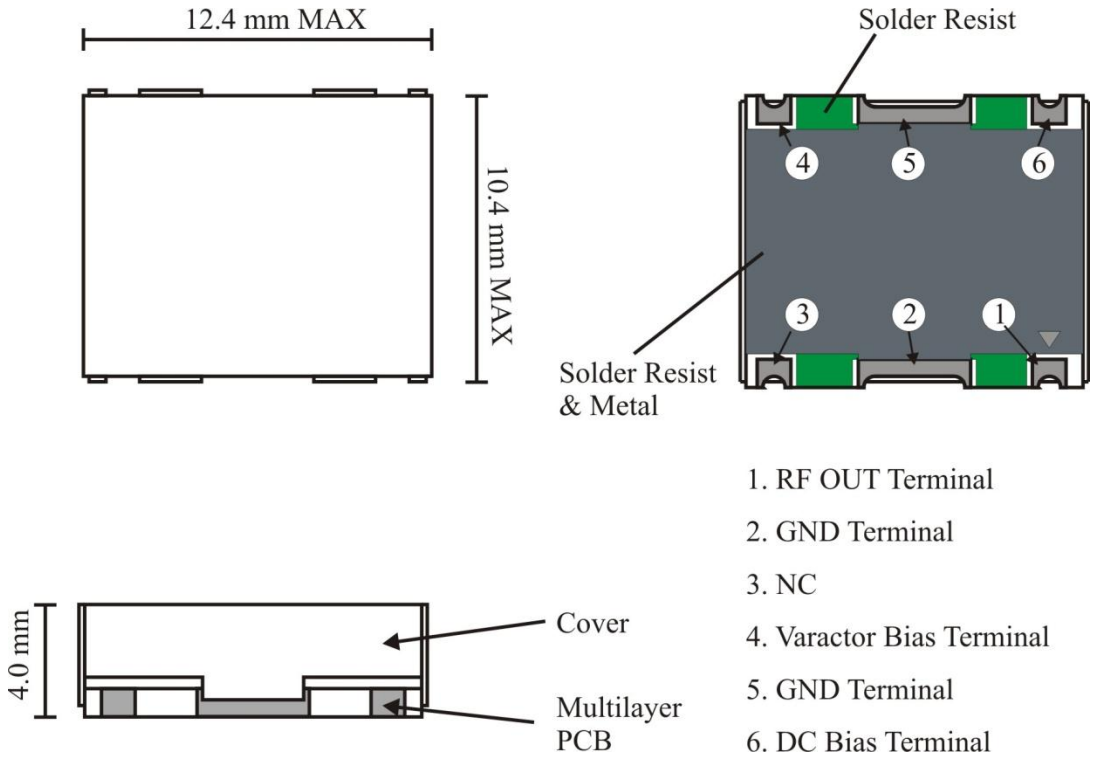


Figure 10.44 Configuration of VCO for Mobile Communication

Fig. 10.45 shows the cross-sectional view of the multilayer PCB. The substrate is composed of a three dielectric sheets of FR4 and the total thickness is 1.0 mm. Each dielectric has equal thickness. The first metal layer is for components mounting and the second metal layer is for the ground, providing grounding for the first metal layer. The third metal layer is for the RFC, strip line resonator, and connection lines and the fourth metal layer is also used as the ground. Thus, the lines on the first layer is considered as microstrip lines from the electromagnetic point of view and the lines on the third layer become striplines since both sides are surrounded by the ground plane. Note that except for the connecting holes, the lines on the first and third layers are electromagnetically isolated due to the second and fourth layers.

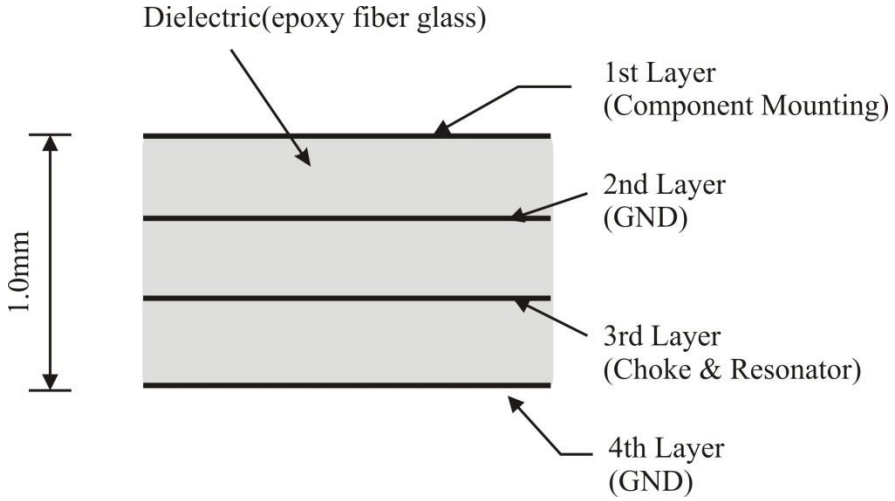


Figure 10.45 Configuration of Multilayer Printed Circuit Board

The VCO circuit used here is shown in Fig. 10.46. In Fig. 10.46, two transistors Q_1 and Q_2 are connected in cascade. Transistors Q_1 and Q_2 use a common emitter current and the VCO consumes only about 1/2 of DC current compared with other VCOs not using cascaded structure. However, relatively low DC voltage is assigned to between the collector-emitter of transistors Q_1 and Q_2 and significant distortions can occur even at a low RF output power as well as at high output power which is a disadvantage.

In Figure 10.46, resistors R_1, R_2, R_3, and R_E determine the DC base voltages of Q_1 and Q_2 and the emitter current of transistor Q_1 and Q_2. Supply voltage is divided by resistors R_1, R_2, and R_3. The DC voltage across resistor R_3 is applied to the base of transistors Q_1. From this DC base voltage, the emitter current of transistor Q_1 can be controlled by varying the value of resistor R_E. In addition, this current becomes the emitter current of transistor Q_2. As the impedances of these resistors can be set higher than those of their surrounding components, they can be neglected at the oscillation frequency. Generally, in the frequency band of operation (800 MHz ~ 2 GHz), the Q of chip capacitor is higher than that of an inductor. Also because of their small sizes, chip capacitors are mostly employed to construct VCO circuit. Inductors are used for RFC and a resonator in the form of short transmission line. The collector of transistor Q_1 is connected to ground through bypass capacitor C_{B2}, and the transistor Q_1 operates as common-collector. The capacitor C_E is a feedback capacitor to yield the negative resistance. When the value of the feedback capacitor C_E is small, only the resistor R_E is left at the emitter of Q_1, which becomes a negative feedback circuit consisting of resistor R_E. As a result, the negative resistance disappears. In addition, when the value of C_E is too large, capacitor C_E operates as a short. Thus transistor Q_1 operates as a common emitter and

negative resistance is also not induced. Thus, in order to induce negative resistance, the value of the feedback capacitor C_E must be appropriate at the operating frequency. That is, under these conditions, ignoring R_E and C_{c2}, the impedance looking into the base of the transistor Z_t can be written as

$$Z_t = \frac{1}{j\omega\left(C_E \,||\, C_{be1}\right)} - \frac{g_{m1}}{\omega^2 C_{be1} C_E} \tag{10.52}$$

Here, C_{be1} and g_{m1} represent the base-emitter capacitance and trans-conductance of Q_1. Oscillation is possible due to this generated negative resistance.

The oscillation output appears across capacitor C_E, which is applied to the base of transistor Q_2 through capacitor C_{c2}. The transistor Q_2 operates as common emitter due to the bypass capacitor C_{B2}. Thus, transistor Q_2 operates as an amplifier, the oscillation output which appears across capacitor C_E is amplified by transistor Q_2, which is then output to the load. The chip inductor L_1 connected to the collector of the transistor Q_2 is an RFC and capacitors C_{m1}, C_{m2} are for matching which ensures maximum power is delivered to the load. Thus, C_E is set so as to generate a negative resistance at the operating frequency and part of C_E is contributed by capacitance C_{c2} connected to the input of transistor Q_2. The lower the value of C_{c2} the lower the power delivered to transistor Q_2 and the larger the value of C_{c2} the larger the power delivered to Q_2 which causes distorted output to appear at the load.

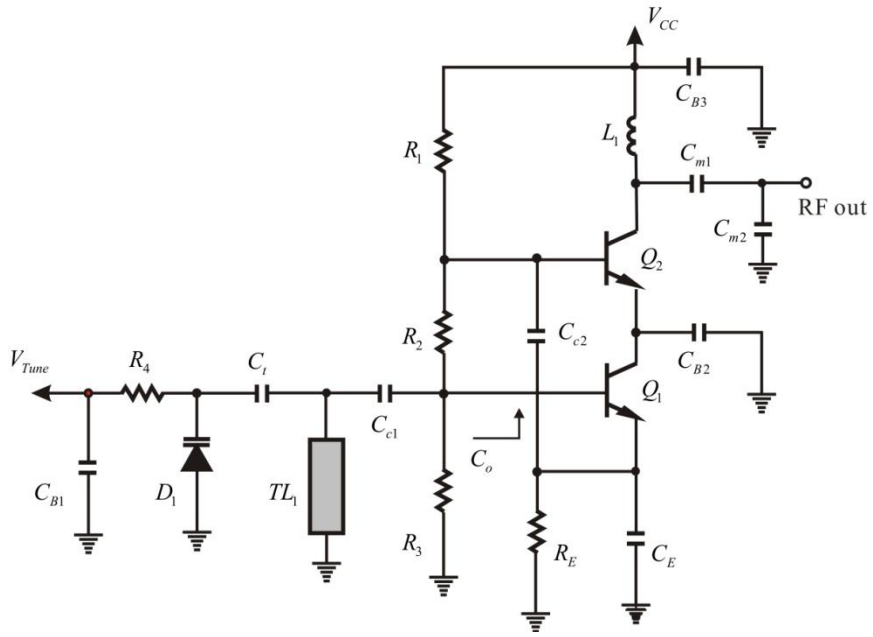


Figure 10.46 Schematic of Voltage-Controlled Oscillator

The resonator in Fig. 10.46 is composed of a short transmission line TL_1, capacitor C_t and varactor diode. The resonant frequency of the resonator is tuned through a varactor diode. Such capacitance tuning range of the varactor diode is limited by the added C_t. Thus the oscillation frequency tuning range can be adjusted by controlling capacitor C_t. The oscillation frequency tuning

range is reduced compared with direct oscillation frequency tuning using varactor diode alone but the Q of the resonator becomes higher due to the added C_t.

Capacitor C_{c1} is added in series to the base of the transistor Q_1, and the imaginary part of the impedance generated by the feedback capacitor C_E can be changed. This makes it easy to tune out the inductance of the resonator at the oscillation frequency. Through this, the resonator and active part can be in series resonance at the frequency of oscillation.

In summary, the function of the capacitor C_t is related to the oscillation frequency tuning range, the capacitors C_{c1} and C_E are associated with the oscillation formation, and C_{c2} is related to coupling of the oscillation power and delivery to the amplifier. Capacitor C_{c1} and inductor TL_1 determine the oscillation center frequency of the oscillator. In particular, by varying the value of inductor TL_1, it is possible to easily adjust the oscillation center frequency to some extent. In the case of capacitor C_{c1}, when considered in series, it does not change the negative resistance but when considered in parallel, it gives a variation of negative conductance. Thus, by adjusting capacitor C_{c1}, the oscillation may disappear. Therefore, TL_1 is efficient for tuning the oscillation center frequency; however it is difficult to tune once fabricated. Sometimes, by connecting a small tunable capacitor pattern in parallel with TL_1, an adjustment of the inductor value of TL_1 is possible and the oscillation center frequency of the oscillator can be tuned to some extent.

Furthermore, as these components are mounted on PCB in the form of chip components during fabrication, it is easy to modify their values and the exact values of the length and width of the lines are not required as in the case of microstrip oscillator. From this perspective, to design the VCO for mobile communication, the function of each component should be understood and the range of values to satisfy the given specification should be found through design or simulation.

The following, Table 10.1, is a brief specification of the VCO for mobile communication, described above. The transistor used is 2SC4226 from NEC.

Table 10.1 Design specification for voltage-controlled oscillator for mobile communication

Spec Item	Value
Freq. Tuning Range	1720-1780 MHz
DC Supply Voltage	3.3 V
DC Current Consumption	8 mA
RF Output Power	> -3 dBm
Active Device	2SC4226

To design a VCO for mobile communication that satisfies the above conditions, the DC bias must first be set. The circuit of the active part is set up as shown in Fig. 10.48 to determine the DC bias. As all the capacitors used are implemented as chip capacitors, all the chip capacitors are replaced by series RLC equivalent circuit to include the parasitic components as was described in Chapter 2. In Fig. 10.47, from a 3.3V power supply, the base voltage of the oscillating transistor is set using resistors.

$$V_B \cong \frac{R_3}{R_1 + R_2 + R_3} V_{CC} = 3.3 \frac{3.3}{2.7 + 2.7 + 3.3} = 1.25 \text{ V}$$

In addition, the emitter current can be seen to be

$$I_E = \frac{V_B - 0.7}{R_E} = \frac{1.25 - 0.7}{50} = 11\text{ mA}$$

This can be seen to be similar to the value of the current, set as the goal. The exact value is evaluated through DC simulation. The calculated DC collector current can be seen to be 6.45 mA at a supply voltage of 3.3 V and the supply current is 6.83mA which satisfies the goal of 8 mA.

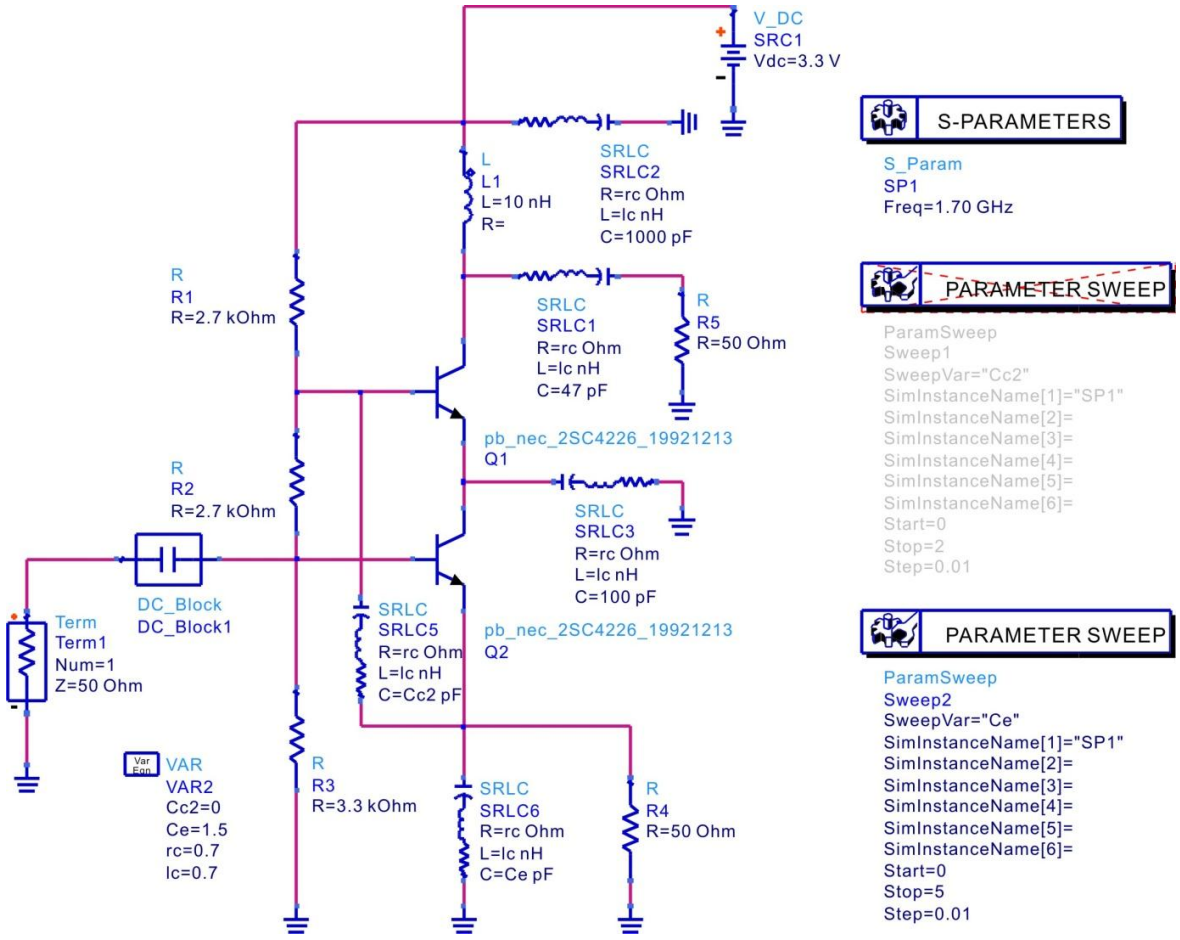


Figure 10.47 Circuit for Determining C_e and C_{c2}

Next, in order to operate the oscillating transistor (transistor Q_2) in common collector mode, the value of DC block capacitor is set to100 pF, the bypass capacitor value to 1000 pF, the value of the RF output DC block capacitor to 47 pF, and no output matching circuit is used. Furthermore, the RFC was determined to be a 10 nH chip inductor (approximately 100 ohms at the oscillation frequency).

As mentioned earlier, the magnitude of the negative resistance is determined by the feedback capacitor **Ce** and the coupling capacitor **Cc2**. To determine these values, firstly, **Cc2** is set to 0 and the magnitude of the negative resistance is calculated by varying **Ce**. The coupling capacitor **Cc1** is replaced by the DC block and the variation in the value of the negative resistance is viewed with respect to **Ce**.

Once set up, the computed results are as shown in Figure 10.48(a). The maximum value of negative resistance can be seen to occur for **Ce** = 1.95 pF. By considering the loading effect of **Cc2**, **Ce** was initially set to 1.5 pF and **Cc2** was varied. When **Cc2** was varied, the magnitude of the negative resistance reduced; this is shown in Fig. 10.48(b). Thus, **Cc2** was selected as 1.2 pF. This is because the oscillation output power may not be delivered to the load for smaller value of **Cc2**.

Next, it is necessary to set up a circuit to investigate the oscillation frequency tuning range for the values thus set. The **smv1235-079** varactor diode was used. The equivalent circuit of this varactor diode is as shown in Fig. 10.49. Notably, as the capacitance of the varactor diode from 0V is large, the varactor diode will practically operate as a variable inductor. The equivalent circuit configured in Fig. 10.49 is made a sub-circuit in the oscillator circuit that is set up to investigate the frequency tuning range of the circuit in Fig. 10.50.

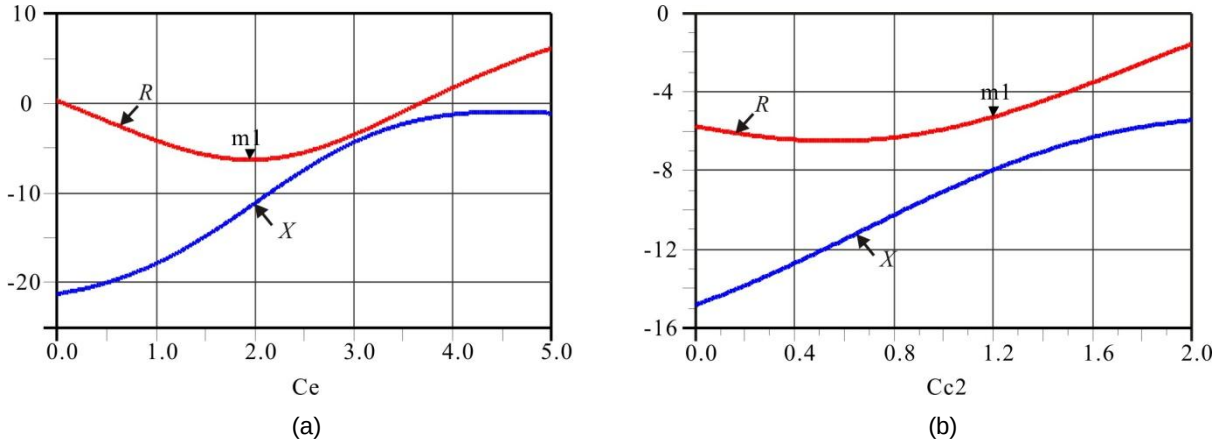


Figure 10.48 Determination of C_e and C_{c2} values by simulation

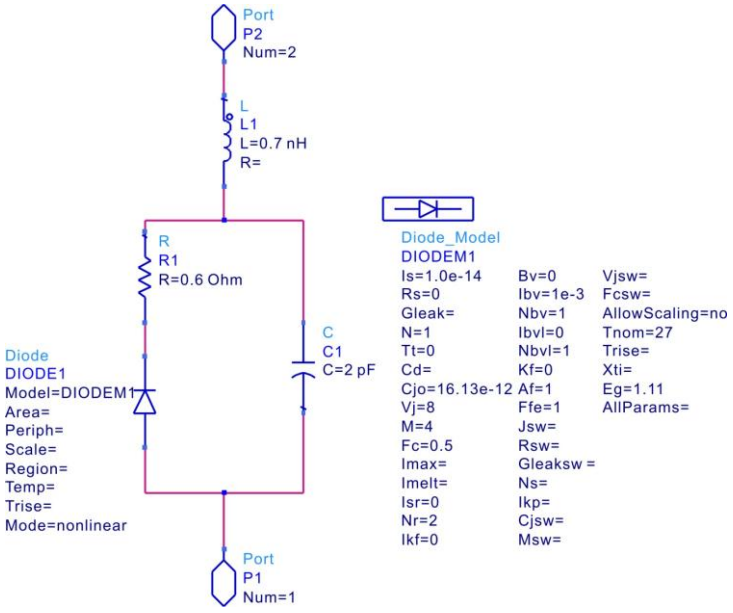


Figure 10.49 The equivalent circuit of varactor diode

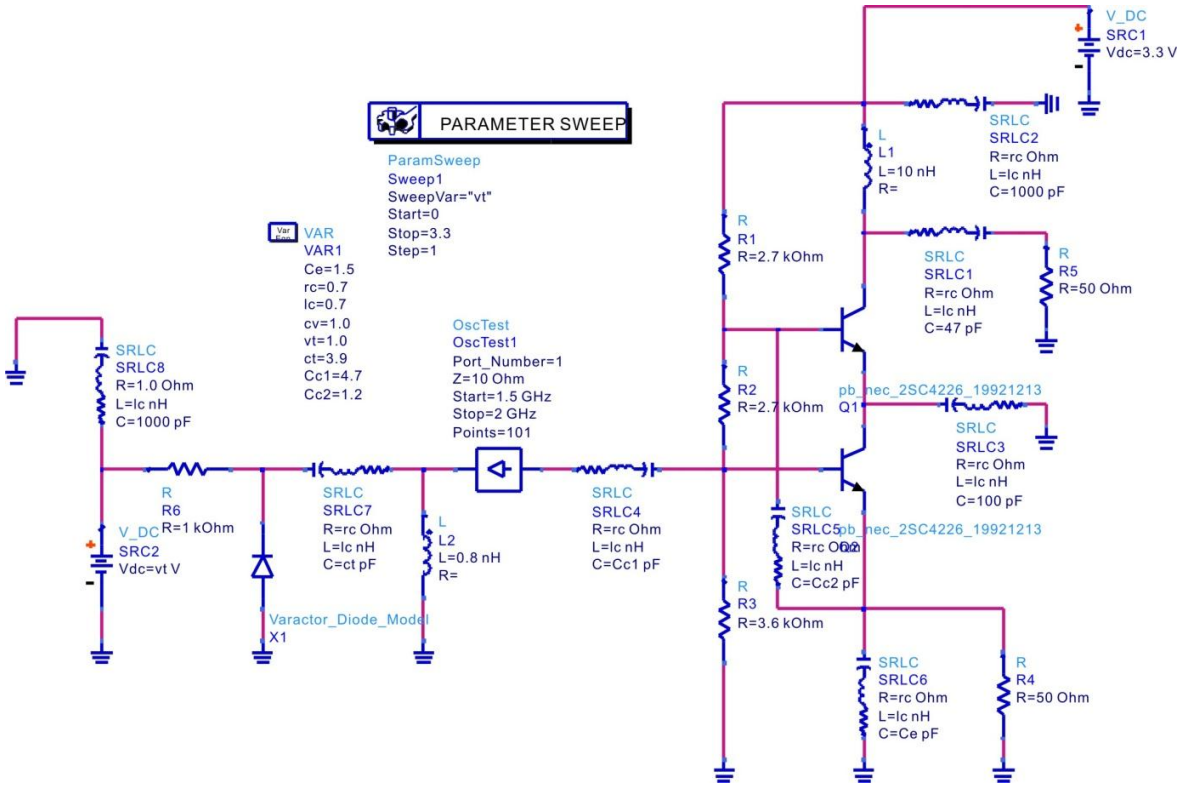


Figure 10.50 VCO circuit for the simulation of oscillation frequency tuning range.

As shown in Fig. 10.50, the inductor in the resonator was set to 0.8 nH. The tuning voltage of the varactor diode is changed from 0 to 3.3V, and the values of the capacitors **Cc1** and **Ct** were then adjusted. The oscillation center frequency is moved using **Cc1** and the oscillation frequency tuning range was adjusted using **Ct**. Through the adjustment, the value of **Cc1** was set to 4.7pF and **Ct** was set to 3.9 pF. Figure 10.51 is the simulation results using **OscTest** and shows the magnitude and phase changes of S_{11} with respect to frequency. From this result, the frequency tuning range is about 1.700 ~ 1.770 GHz and can be seen to meet the specifications.

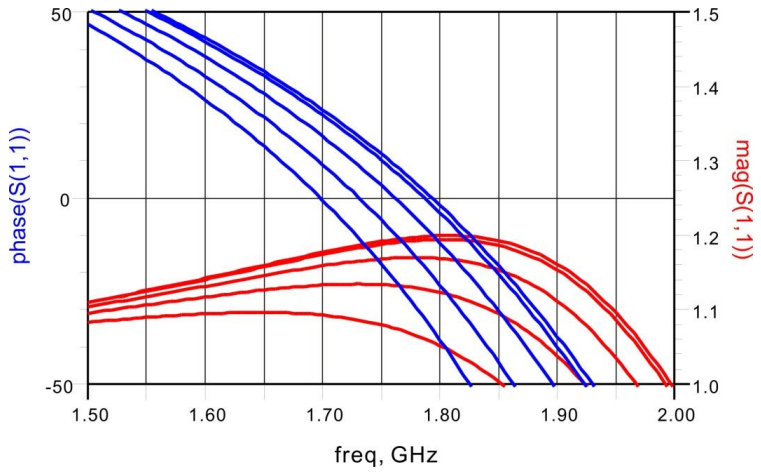


Figure 10.51 Frequency Tuning Range of VCO circuit

Oscillation can thus be seen to occur within the oscillation frequency range that is obtained at small-signal. Next, the circuit shown in Fig. 10.52 is set up and large-signal simulation is performed in order to investigate the output power and frequency tuning range at large-signal. The simulation results of the circuit in Fig. 10.53 are shown in Fig. 10.54, and as can be confirmed from Fig. 10.53, the output of -1.698 dBm ~ -0.690 dBm meets the desired specifications. The value of tuning voltage **Vt** which outputs the desired oscillation frequency tuning range can be seen to be approximately 0.6 V ~ 2.8 V.

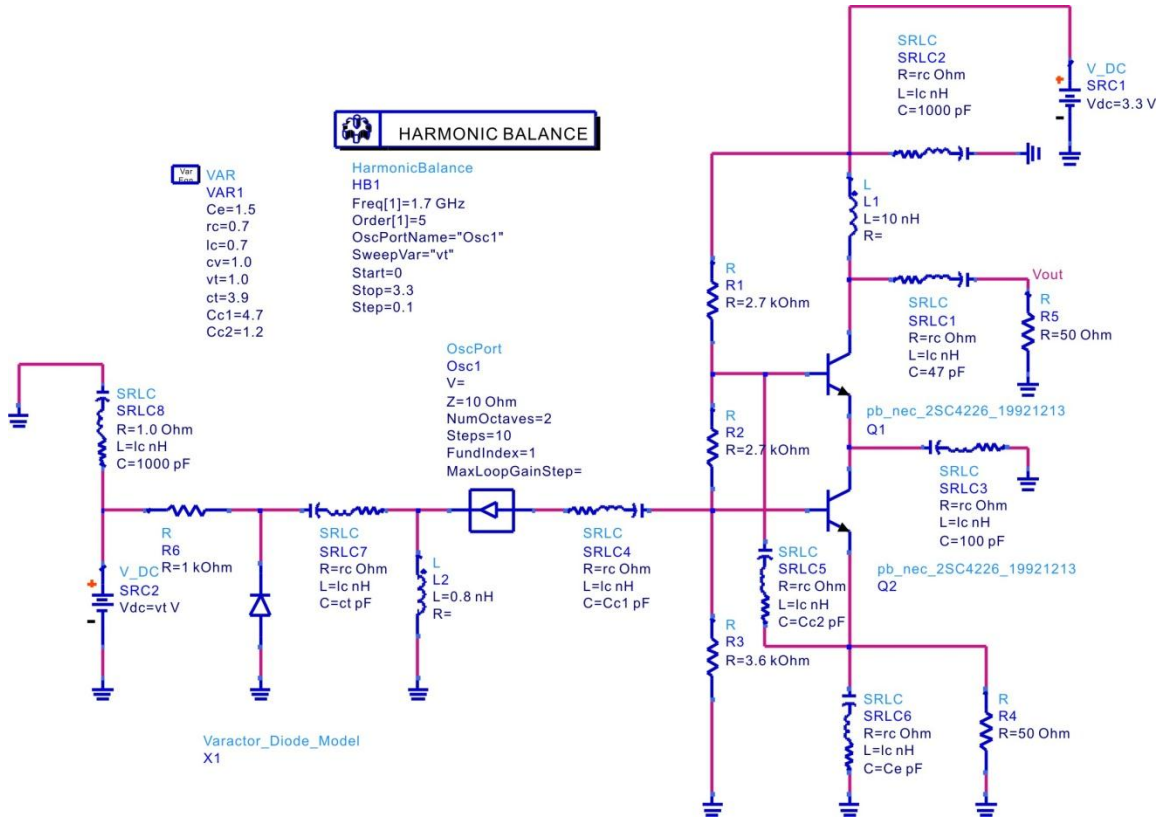


Figure 10.52 Circuit for large-signal simulation

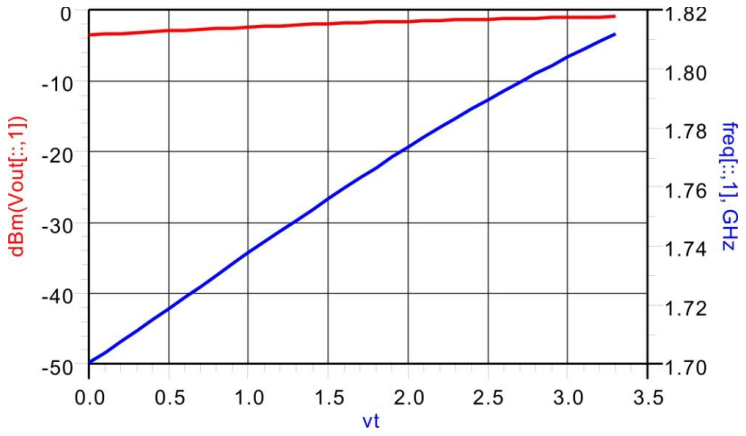


Figure 10.53 Oscillation frequency and output variation with respect to tuning voltage Vt

In Fig. 10.54(a), the time domain waveform is shown with the tuning voltage **Vt** as a parameter and the output waveform can be seen to be close to a sinusoidal waveform. The spectrum of the oscillation waveform is shown in Fig. 10.54(b) and the second harmonic is found to be suppressed by approximately -20 dBc compared with the fundamental.

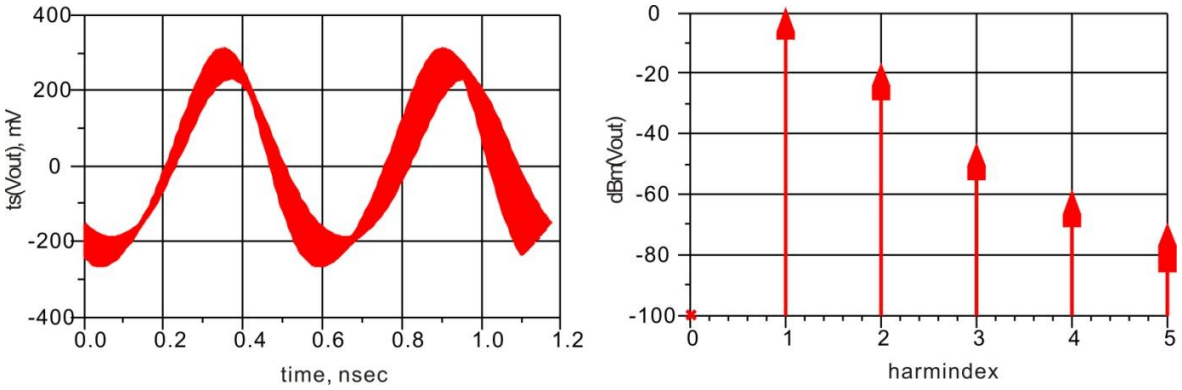


Figure 10.54 Output (a) waveform and (b) spectrum

10.5.2 Design of Microstrip Oscillator

The technique employed in the design of the VCO for mobile communication described earlier is useful when components can be easily be connected and removed by soldering. Identifying the role of each component in the circuit enables the oscillator to be designed and fabricated to meet specifications by adjusting the values of the components through soldering rather than employing the exact values of the components required in the design. On the other hand, since the microstrip oscillator to be described in this section is mainly consists of microstrip lines, it is not easy to adjust microstrip lines as is done in the VCO for mobile communication. Thus, the exact dimensions of the microstrip lines are necessary in the design of a microstrip oscillator.

The microstrip oscillator can be designed using the impedance method as in the design of the VCO for mobile communication described in previous sections. In this section however, we will demonstrate the design using the method of Example 10.13. The transistor used for the design, a FHX35LG packaged as shown in Fig. 10.56. The large signal model of this transistor is available in ADS. This section looks at the design of the oscillator using the large signal model of the FHX35LG. Typically, the large-signal model shows some errors as previously discussed in Chapter 5 and the error becomes even larger as the frequency increases. Taking this into consideration, the oscillation frequency is set at 2.5 GHz which is relatively low.

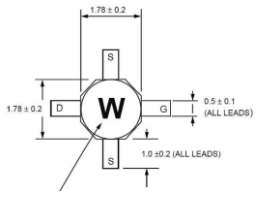


Figure 10.55 FHX35LG transistor geometry

10.5.2.1 Setting of DC Operating Point

Figure 10.56 is a schematic for the simulation of the DC characteristics of the FHX35LG device. To see the DC characteristics, V_{DS} is varied from 0 ~ 3Vand V_{GS} is varied from –0.7~ 0 to examine the drain current I_D. The result is shown in Fig.10.57.

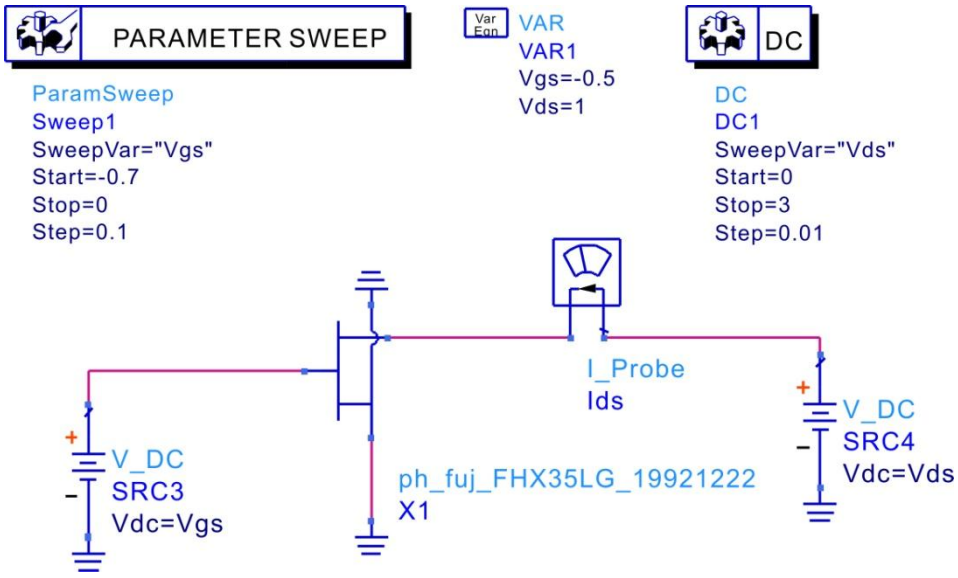


Figure 10.56 DC simulation of FHX35LG

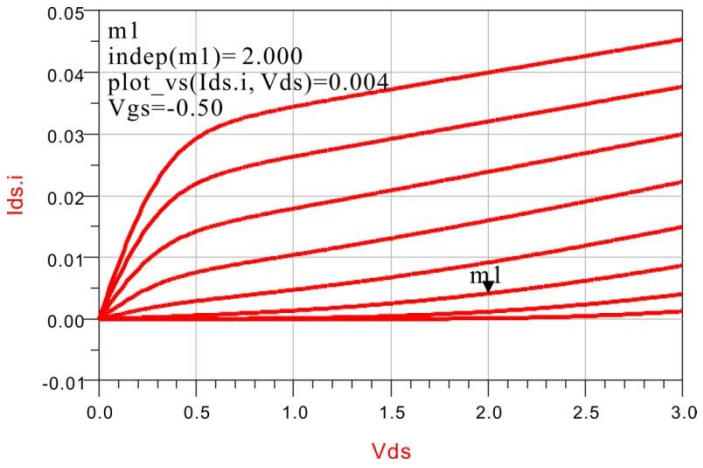


Figure 10.57 Simulated drain current

In Fig. 10.57, the drain current can be seen to be about 4 mA when V_{DS} = 2V and V_{GS} = – 0.5V. In this design, the DC operating point of the oscillator is set to V_{DS} = 2V, V_{GS} = – 0.5V. Such a DC operating point for the oscillator circuit can be achieved using two independent DC supplies for V_{DS} and V_{GS}; however the same DC operating point can be achieved with a single DC supply using a self-bias method. In this oscillator circuit design, the self-bias method is selected for convenience. Thus, a resistance of R_s= 0.5*V*/4mA = 125 ohm is connected to the source terminal with the gate terminal grounded since the value of the gate voltage that gives a drain current I_{DS} = 4 mA is V_{GS} = –0.5V. This yields the source voltage of 0.5V at a drain current of 4 mA and a 2.5 V DC voltage is applied to the drain terminal in order to preserve V_{DS} = 2V.

10.5.2.2 Load-Pull

Figure 10.58 is a schematic of a load-pull simulation for obtaining the load impedance giving maximum output power for the self-biased FHX35LG device. This is set up in the same manner as described in Chapter 9 for power amplifier. The only difference is that the FHX35LG device is self-biased. It is worth noting that, this self-bias method results in a decreased output power, compared to using two DC supplies for the bias. The DC drain current increases in large-signal operation. The increased drain current reduces V_{DS} thereby resulting in a reduced output power. Furthermore, since a part of the output power P_L is fed back to supply input power P_{in} in the oscillator circuit, the oscillator output power becomes P_L–P_{in}. Therefore, the load impedance will need to be set to make P_L–P_{in} maximum. However, since P_{in} is fixed, the maximum of P_L–P_{in} occurs at maximum P_L. Therefore, the problem reduces to the selection of the optimum input power P_{in} to make the oscillation output maximum. Since the optimum P_{in} is unknown, an appropriate value of P_{in} is initially selected and the load impedance giving maximum P_L is obtained. After this, P_L–P_{in} is plotted with the load impedance fixed, from which the optimum P_{in} can be obtained. For this P_{in}, a new load impedance can be computed again through load-pull simulation. These steps are repeated to obtain the optimum load impedance that maximizes the oscillation output.

Another problem is, in order to deliver the maximum input power to the input of the active device, the source impedance and the input impedance of the active device must be conjugate matched. However, the large signal input impedance of the active device is unknown. Therefore, an initial value of the source impedance is determined using the small-signal S-parameters S_{11} and the load-pull simulation is then performed. The large-signal input impedance can then be obtained from the results of the load-pull simulation which is used again in a repeated load-pull simulation. The –1 dBm input power and input impedance **z1** = 6.22 + *j*142 in Fig. 10.58 are the values determined through the repeated process described above. It must be noted in addition that, the 2nd harmonic and 3rd harmonic load impedances were set as 0 and 1 kohm, respectively. This is the same load condition as for class-F power amplifier. Such class-F load condition must be implemented in designing oscillator. However, in order to avoid complexity, the harmonic impedances are not considered in the implementation of oscillator design.

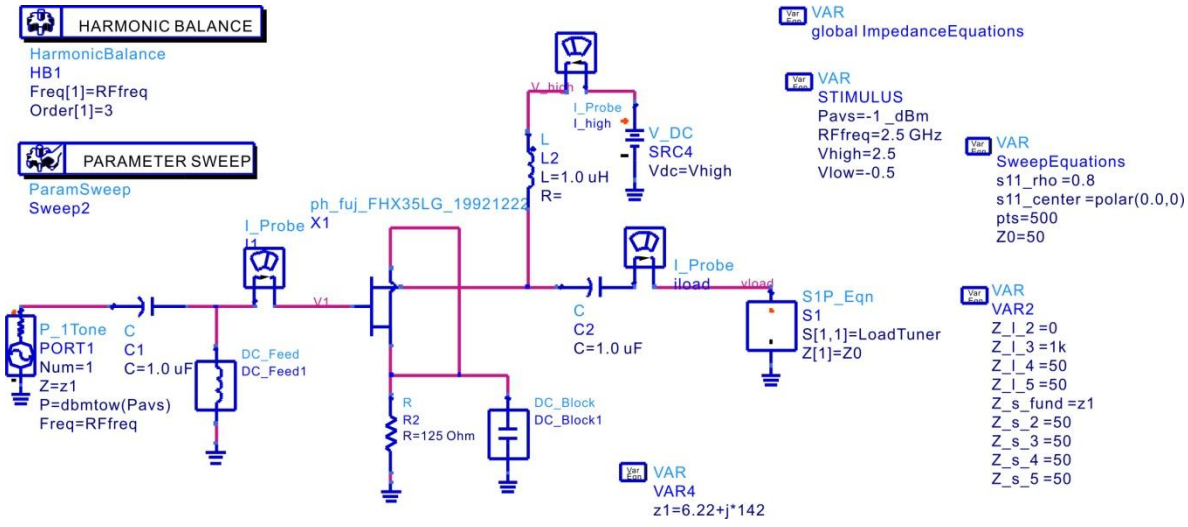


Figure 10.58 Load-pull simulation schematic

Figure 10.59 shows the load-pull simulation results. In Fig. 10.59 when the load impedance is 61.317 + *j*12.761, the obtained output can be seen to be 8.32 dBm. The next step will be the determination of the series feedback circuit of the oscillator using the computed source impedance of 6.22 + *j*142 and load impedance of 61.317 + *j*12.761.

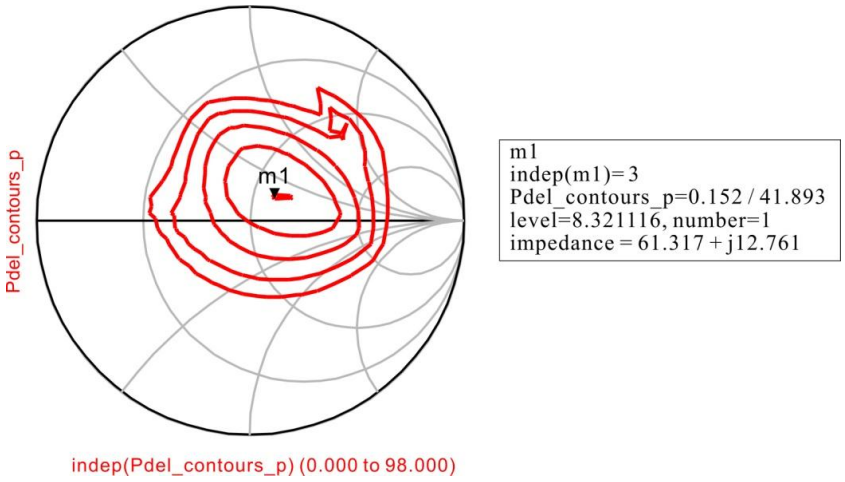


Figure 10.59 Load-pull simulation results

10.5.2.3 Implementation of Series Feedback Network

Given the input power and source and load impedances, the values of the series feedback network of the oscillator can be determined using the method of Example 10.13. The simulation schematic shown in Fig. 10.60 is set up to determine the input current and voltage as well as the output current and voltage.

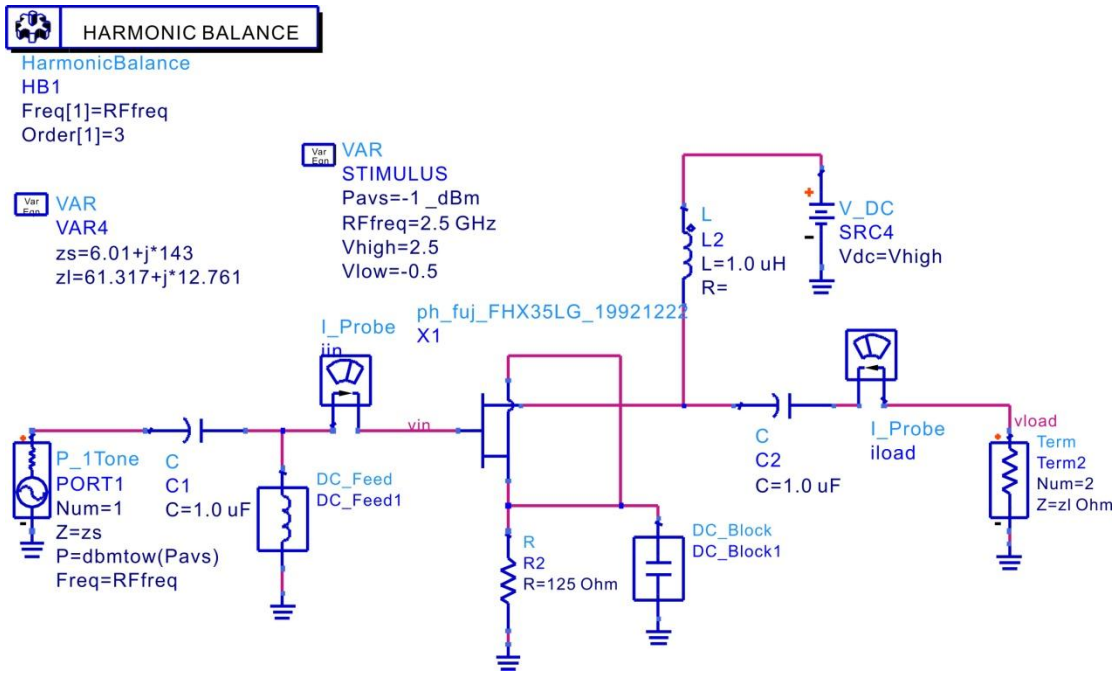


Figure 10.60 Simulation schematic for determining the values of the series feedback network of the oscillator

For the circuit having been set up as shown in Fig. 10.60 and the simulation is performed. The following equations are inserted in the Display window to define the parameters required to compute the values of the series feedback network from the results obtained in the simulation.

```
Eqn I2=-iload.i[1]
Eqn I1=-iin.i[1]
Eqn V1=vin[1]
Eqn V2=vload[1]
Eqn z1=V1/I1
Eqn z2=V2/I2
Eqn beta_f=(1+I2/I1)
Eqn beta_b=(1+I1/I2)
```

The following equations are also inserted in the Display window to determine the values of x, y and Z_L of the series feedback network from the parameters defined above using equation (10.48).

```
Eqn ZL=z2+j*beta_b*real(z1)/imag(beta_f)
Eqn y=-real(z1)/imag(beta_f)
Eqn x=imag(z1)+real(beta_f)*real(z1)/imag(beta_f)
```

The computed results for x, y and Z_L are 148.14, –7.996, and 52.791+j16.008, respectively. In order to verify the results thus calculated, the oscillator circuit is set up as shown in Fig. 10.61.

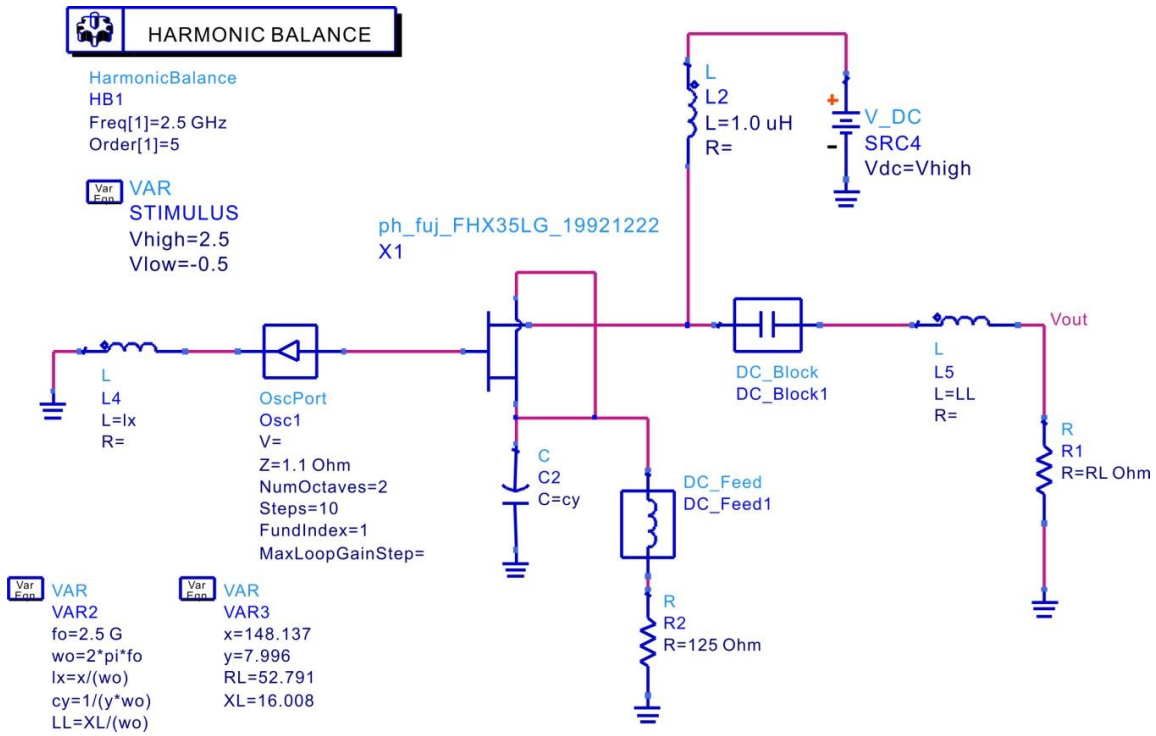


Figure 10.61 Oscillator circuit simulation for confirming the values of the series feedback network

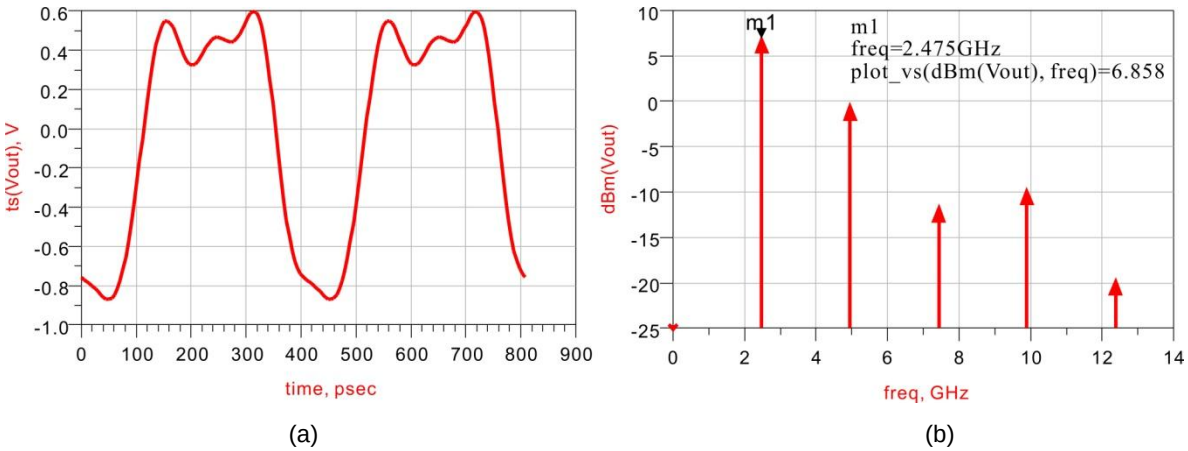
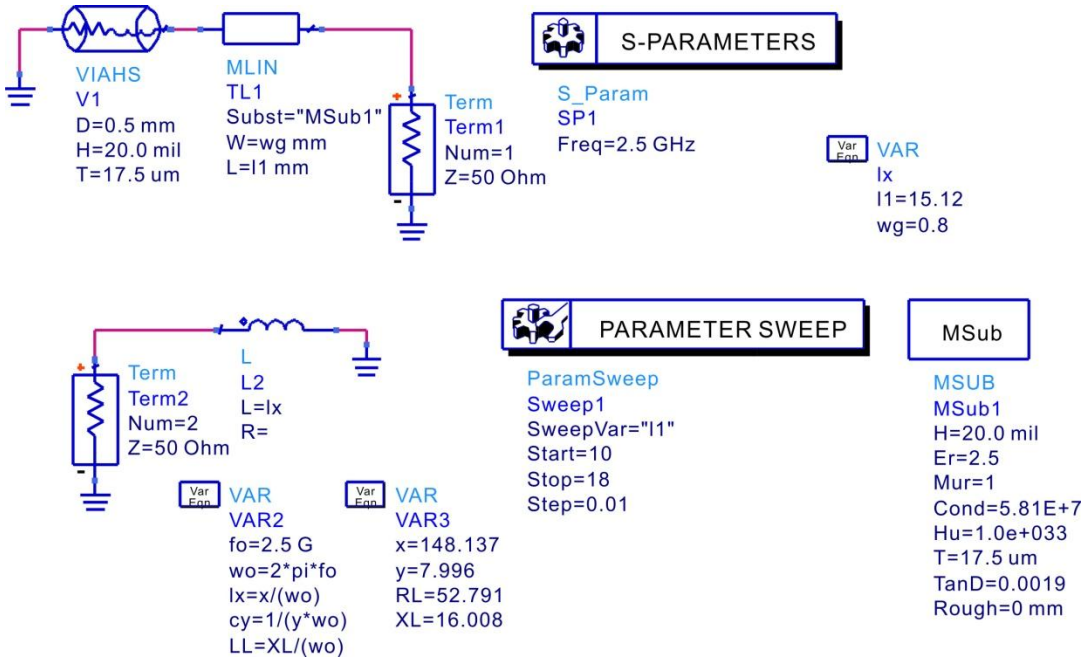


Figure10.62 (a) Oscillation waveform and (b) spectrum obtained through oscillator simulation

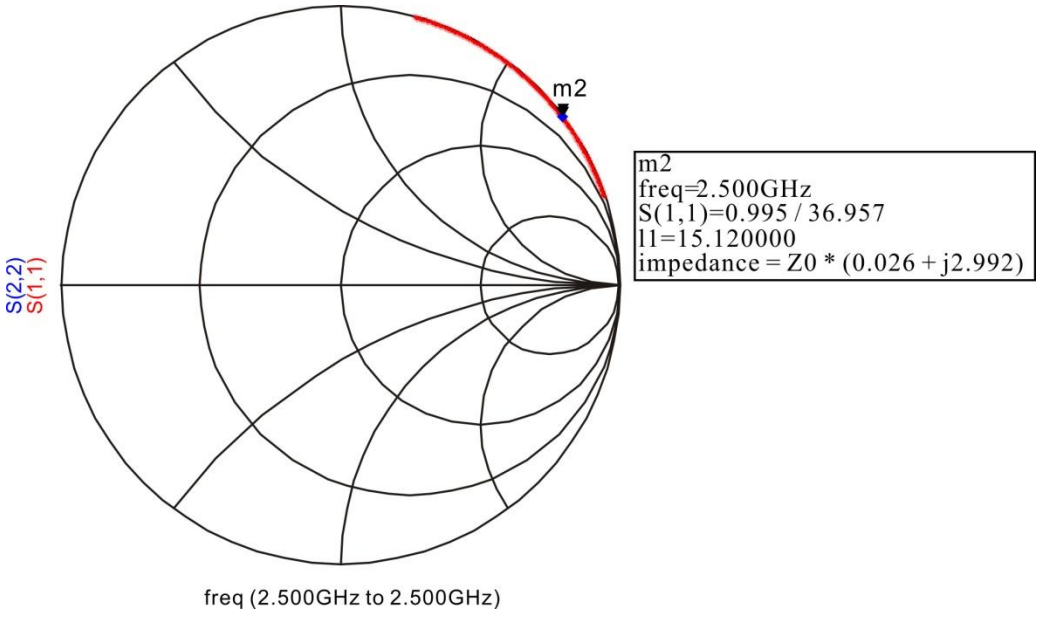
The simulation results for the circuit configured as shown above are shown in Figs. 10.62(a) and 10.62(b). Figure 10.62(a) is the simulated time domain waveform of **Vout** and Fig. 10.62(b) is the spectrum of **Vout**. The oscillation output power can be seen to be approximately 6.9 dBm from Fig. 10.62(b). This can be seen to be less than the 8.3 dBm obtained from the load-pull simulation in Fig. 10.59. Considering the input power is –1 dBm, the oscillation output should be approximately $10^{0.83} - 10^{-0.1}$ = 6mW = 7.7 dBm. Thus, the oscillation output can be seen to have reduced by 7.7–6.9 = 0.8 dBm. Furthermore, the oscillation frequency even though close to 2.5 GHz has slightly reduced to 2.475 GHz. Such difference in the oscillation output and frequency is believed to be due to the fact that the oscillator circuit in Fig. 10.61 does not have the class-F load impedance employed in the load-pull simulation. The load impedance was set as class-F in the load-pull simulation whereas the load impedance of the oscillator circuit is not exact class-F load impedance. However, it can be seen that the result is fairly close to the expected value. It is possible to tune the values of *x* and *y* in order to obtain the exact oscillation frequency, but such tuning is not separately carried out in this example.

10.5.2.4 Implementation of Microstrip Oscillator

The oscillator circuit of Fig. 10.61 was implemented using lumped elements such as inductors and capacitors. Therefore, to implement the microstrip oscillator, the lumped elements of Fig. 10.61 must be replaced with microstrip circuits giving the same impedance values at the oscillation frequency. Figure 10.63(a) is a microstrip circuit for replacing the inductor connected to the gate. The selected substrate has a thickness of 20 mil, dielectric constant of 2.5, and conductor thickness of 17.5 um; the diameter of the via was fixed as 0.5 mm. To replace the inductor with the same value of microstrip, the length of **TL1**, **l1** is varied to obtain the same value of inductance as for the lumped inductor. The width of **TL1** was fixed as 0.8 mm. Figure 10.63(b) is the result of the simulation. S_{11} represents the reflection coefficient with respect to the change of **l1**, and S_{22} is the reflection coefficient due to inductor **lx**. Thus, the length **l1** that gives the same value of reflection coefficient can be seen to be **l1** = 15.12 mm from Fig. 10.63(b).

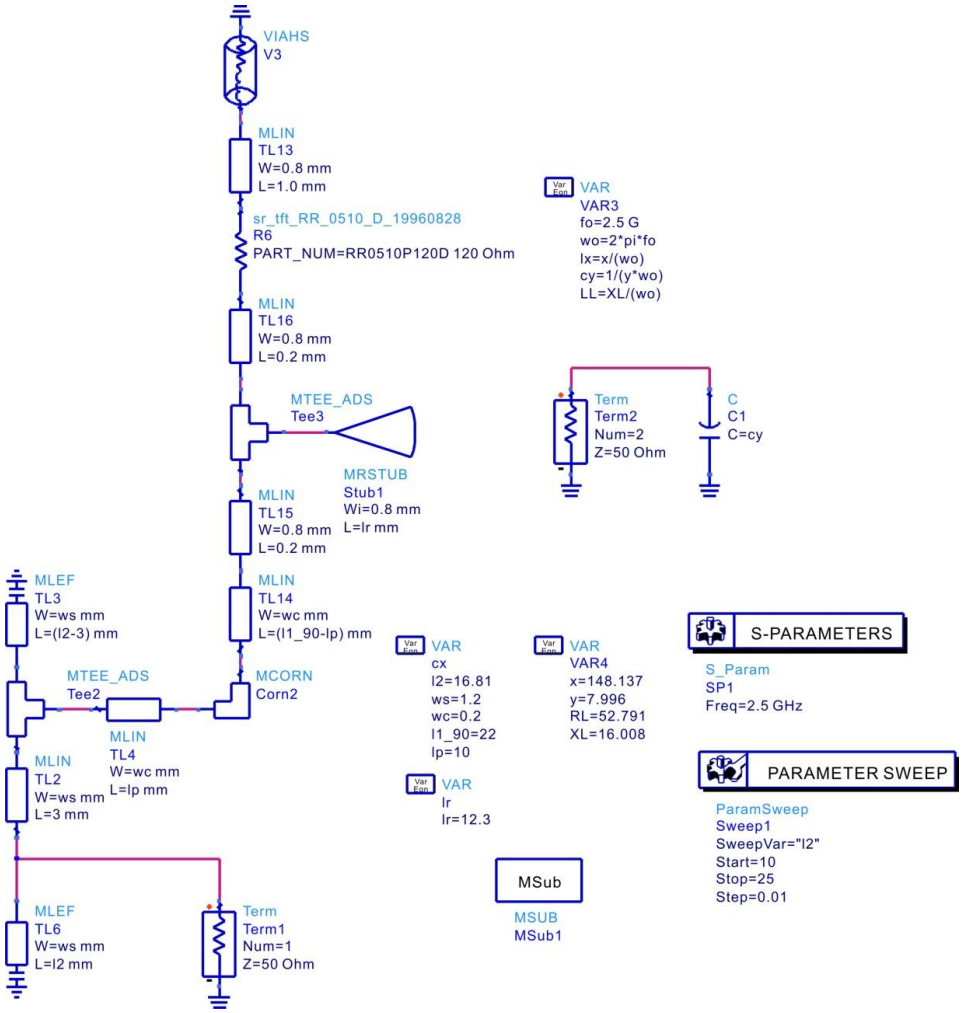


(a)

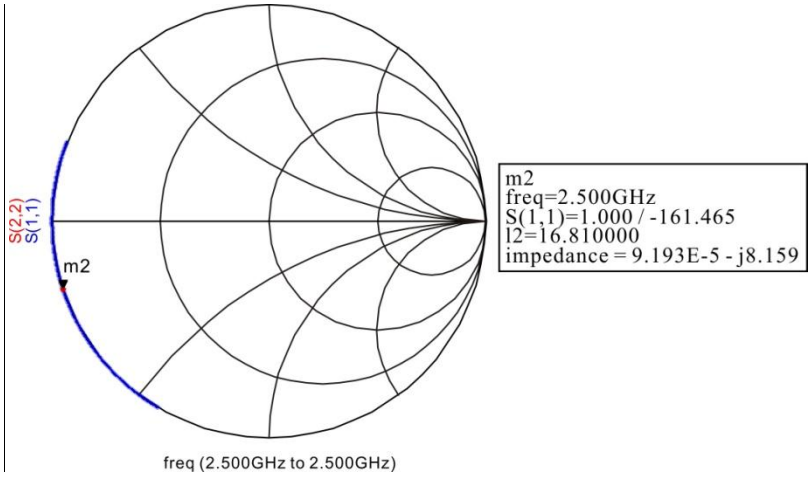


(b)

Figure 10.63 (a) Conversion of gate inductor to microstrip and (b) simulation results



(a)



(b)

Figure 10.64 (a) Microstrip circuit implementation of the feedback capacitor and (b) simulation results

Figure 10.64(a) is a microstrip circuit implementation of the capacitor **cy** which is connected to the source terminal. The selected FHX35LG device has two source terminals. Thus, the capacitor **cy** of Fig. 10.64(a), is configured as the parallel combination of two microstrip circuits as shown in Fig. 10.64(a). Furthermore, the microstrip width is set wider than the width of the source terminal, the value of which is set to 1.2 mm. It is furthermore necessary to include a self-bias circuit. The self bias circuit is included in only one circuit of the parallel combination. The point where the self-bias is connected is set 3.0 mm away from the source terminal. It must be noted that the self-bias circuit has almost no effect on the impedance at the oscillation frequency of 2.5 GHz. The two open microstrip stubs have almost the same impedances at 2.5 GHz because the lengths of the microstrip stubs are set to have equal lengths, **l2**. The length **l2** is adjusted to give the impedance of the parallel combination equal to the impedance of **cy**.

The RFC connected to the source terminal for DC bias consists of a high impedance 1/4 wavelength microstrip line and a radial-stub. The width of the input terminal and angle of the radial-stub is initially fixed at 0.8 mm and 70°, respectively. With this fixed width and angle, the length of the radial-stub is set by separately simulating the impedance of the radial-stub to make the input impedance 0 at 2.5 GHz. The length was calculated to be 12.3mm. The width of the high impedance microstrip operating as RFC was set to 0.2 mm, and the length was set such that, its electrical length is 90° at 2.5 GHz. This value is the **l1_90** in Fig. 10.64(a) which when computed with **LineCalc** can be seen to be approximately 22 mm. The RFC microstrip line is bent at 90° to make the DC biasing easy while maintaining the value of the length **l1_90**. This shape is shown in Fig. 10.64(a). Furthermore, the resistor used in the DC bias was implemented using a chip resistor from the ADS library, and the 120 ohm was selected because the determined value of 125 ohm is not available in the ADS library. The simulation was performed by varying the length **l2**, the results of which is shown in Fig. 10.64(b). From Figure 10.64(b), when **l2** = 16.8 mm, it can see that the impedance of the microstrip is the same as that of the capacitor **cy**.

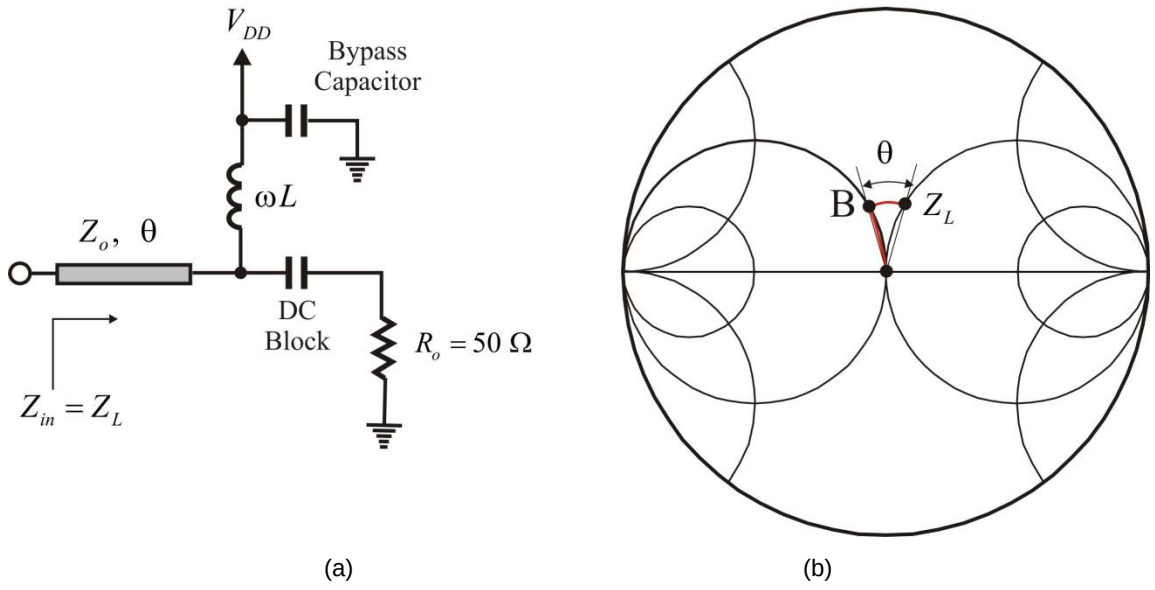
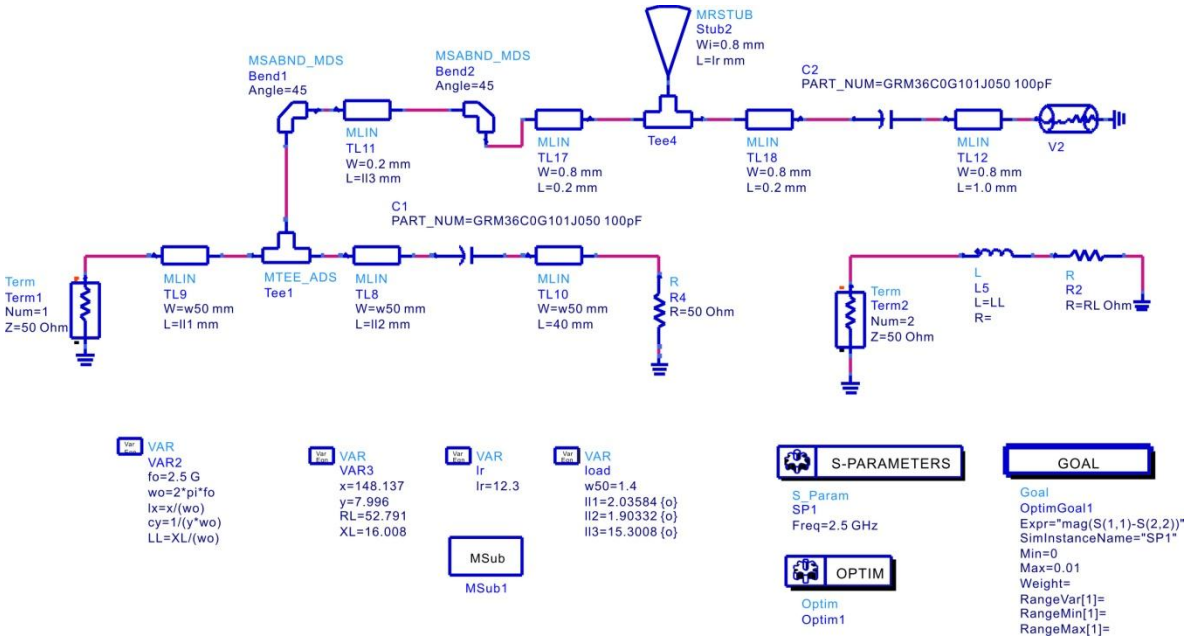
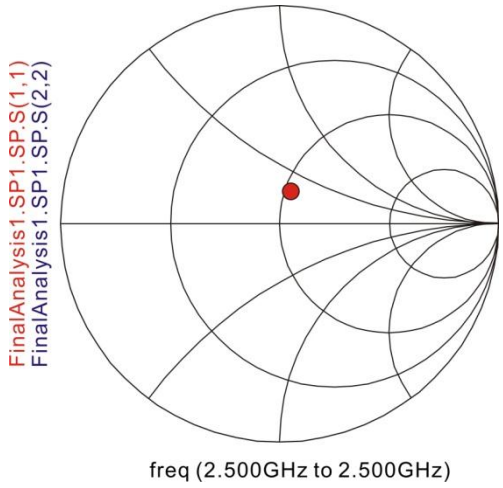


Figure 10.65 (a) Load circuit and (b) matching process



(a)



(b)

Figure 10.66 (a) Load configured as microstrip circuit and (b) the result of the optimization

In the case of the load circuit, the impedance seen from the drain terminal should be implemented to have the impedance Z_L = 52.791 + j16.008. This requires the synthesis of a matching network to transform the 50 ohm load into Z_L. In addition, the load circuit must be implemented to include the DC block and DC supply circuit of Fig. 10.61. Conceptually, such a circuit can be configured by inserting an inductor in parallel and then connecting a 50 ohm transmission line as shown in Fig. 10.65(a). The parallel inductor here can be formed by connecting a bypass capacitor at the end of the high impedance transmission line as shown in Fig. 10.65(a). Thus, the DC supply can be applied through the bypass capacitor and the design of a separate DC supply circuit is not required. The DC block capacitor is implemented with a 100 pF chip capacitor.

As explained in Chapter 2, the chip capacitor is not a pure capacitor. However, in order to show the operation of the circuit of Fig. 10.65(a), the impedance of the chip capacitor is approximated to 0. When the impedance of the 100 pF DC block chip capacitor is considered as 0, for the appropriate inductor value, the parallel inductor moves the 50 ohm load at the origin to the position B as shown in Fig. 10.65(b). The impedance at position B is then moved into the position of Z_L through the clockwise rotation of the 50-ohm transmission line. Thus, the load circuit can be implemented using the circuit shown in Fig. 10.65(a).

Figure 10.66(a) is the load circuit implemented with microstrip. The bypass capacitor for the DC power supply is implemented with a radial-stub and a100 pF chip capacitor. The radial-stub has the dimensions used in the implementation of **cy**. Furthermore, a 100pF chip capacitor is connected in parallel for DC power supply. A microstrip of 0.2 mm width was used for the parallel inductor, the length **ll3** of which is varied to provide the appropriate inductor value. The microstrip line is bent to minimize possible unwanted coupling to the **cy** circuit. The width of the 50 ohm microstrip is approximately 1.4 mm, and its length is set to **ll1** for optimization. Furthermore, variable length of 50 ohm microstrip can also be inserted in front of the DC block chip capacitor. The length of this microstrip **ll2** was optimized together with **ll1** and **ll3**. Figure 10.66(b) shows the optimized impedance for the optimized dimensions shown in Fig. 10.66(a). The impedance can be seen to be close to the desired design value of $Z_L = 52.791 + j16.008$.

A large-signal oscillator simulation was performed using the **lx**, **cy**, and load circuit implemented using microstrip. The simulation shows oscillation frequency of 2.46 GHz and output power of 5.5 dBm. These values are slightly different from those obtained in the circuit simulation, however, as previously mentioned; this can be thought of to be due to the difference in harmonic impedances.

10.5.2.5 EM Simulation

The microstrip oscillator circuit thus implemented fairly accurately predicts the behavior of the actual oscillator; however more accurate values can be determined through EM simulation. Therefore, the values previously determined in circuit simulation can be further refined through EM simulation. The procedure is the same as the previous one. In the case of the gate inductor **lx**, the layout is generated from the previous microstrip circuit using the ADS auto-layout utility and **l1** in the generated layout is specified as a variable for a newly defined *layout component*. By inserting the layout component, thus set, in the Schematic window, the simulation can be performed in the Schematic window as shown in Fig.10.63(a). A slightly changed value of **l1** is obtained as **l1** = 15 mm. Internal ports in Momentum are used for the simulation of the **cy** circuit connected to the source terminal. Such internal ports can cause changes in the locations of the ports when the lengths of transmission lines defined as variables change. There are several techniques for solving this problem, in this design however, a fixed length microstrip in a layer which has no function is used to connect the internal ports thereby eliminating the changes in the locations of the ports due to the length changes. Also noteworthy is that, the accuracy of the ADS internal port is currently not well known. Using Sonnet for the EM simulation is recommended for higher accuracy. A length **l2** = 17.1 mm was obtained through this EM simulation. Compared to the circuit simulation, the length **l2** differs by about 0.3 mm from that of the circuit simulation. The lengths of the microstrip lines in the load circuit connected to the drain terminal are also determined in a similar way through optimization in EM simulation. The computed values were obtained as **ll1** = 2.99 mm, **ll2** = 0.04 mm, and **ll3** = 9.30 mm. The values obtained in the EM simulation can be seen to be significantly different from those obtained in the circuit simulation and of Fig. 10.66.

Figure 10.67 is the schematic of the oscillator whose dimensions were tuned through the EM simulation described above. The RFCs, DCFEED1 and DCFEED2, and DC block, DC_Block1 in Fig. 10.67 are used for computational efficiency. Without such RFCs or DC block, the EM simulation is extended up to DC simulation, which significant increases the computation time beyond what is tolerable. This also degrades the accuracy of the computation in DC. It must however be noted that, such RFCs or DC block inserted in the circuit have no effect on the computation at DC. To this end, the frequency range of the **lx** and load circuit as layout component was set to 1 GHz to 15 GHz.

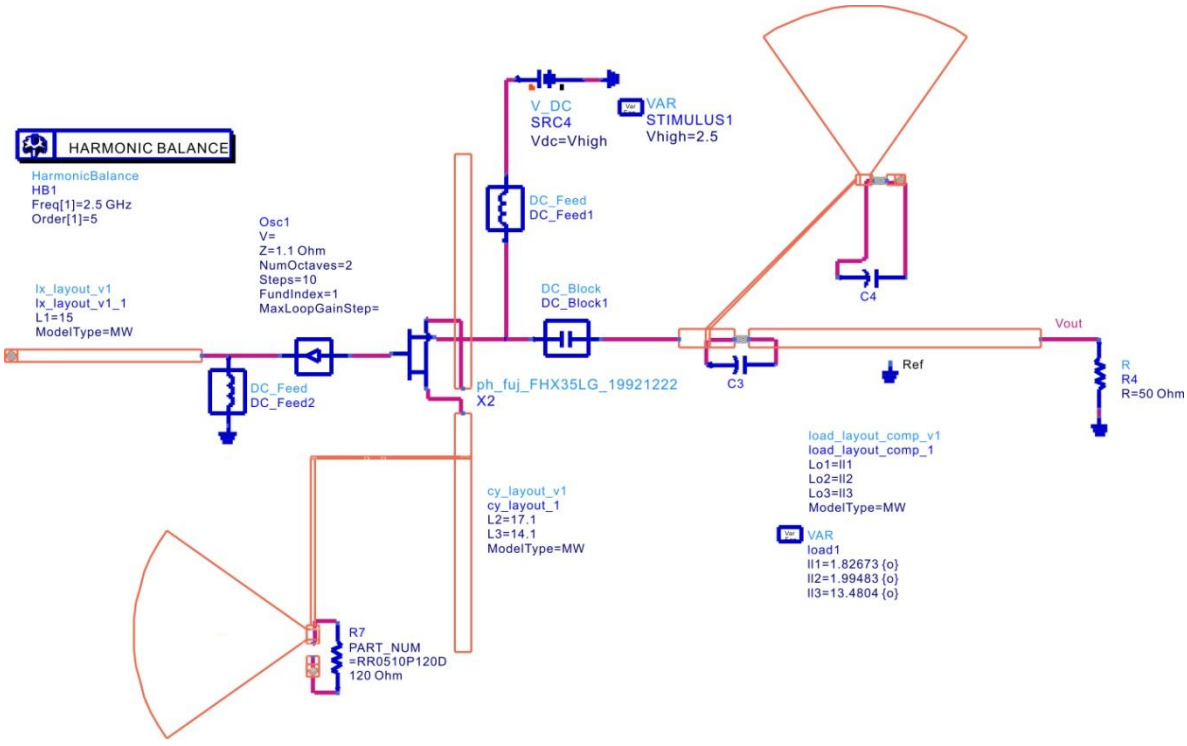
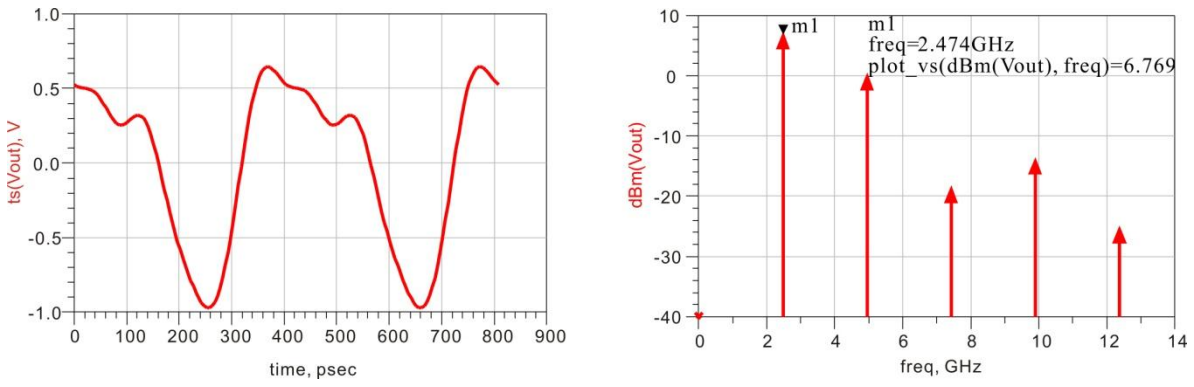


Figure 10.67 Large-signal simulation of microstrip oscillator circuit through EM simulation



(a) (b)

Figure 10.68 (a) Waveform and (b) spectrum from the EM simulation

The simulation results are shown in Fig. 10.68. Figure 10.68(a) shows the oscillation waveform obtained from the EM simulation. The spectrum of the oscillation output is shown in Fig. 10.68(b). The oscillation frequency and output power in Fig. 10.68(b) are 2.474 GHz and 6.796 dBm respectively, values that are close to those in the circuit design.

The oscillation frequency can be tuned to the design frequency of 2.5 GHz by varying **cy** or **lx**. When **lx** connected to the gate is varied and the length variable of **lx**, **l1** is set to **l1** = 14.75 mm, a value close to the desired oscillation frequency of 2.5 GHz can be obtained. Figure 10.69 shows the layout of the microstrip oscillator designed as such.

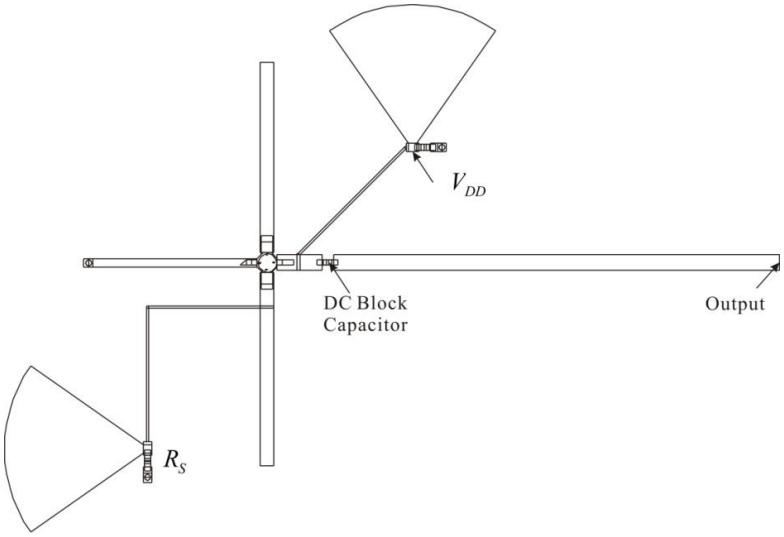


Figure 10.69 Microstrip oscillator circuit layout

The layout of the microstrip oscillator shown here is determined by computing the variables of the layout components **lx**, **cy**, and load circuit through independent EM simulations. This is done for the ease of the calculation. Undesired coupling may exist between **lx**, **cy**, and the load circuit. The radial-stubs of the load circuit and **cy** circuit in Fig. 10.69 are quite close which requires more accurate calculation. In addition, it can be seen that the bias circuit of the **cy** and **lx** circuits are close. This can also cause unwanted coupling. To consider such coupling, the gate, drain and source terminals of the FET must be set as internal ports, and the EM simulation of the external circuit, **lx**, **cy**, and the load circuit performed for such defined internal ports. However, since this simulation is not a new process, it can be done by following the previous EM simulation procedure.

10.6 DIELECTRIC RESONATOR OSCILLATOR

10.6.1 Operation of Dielectric Resonator (DR)

Dielectric resonator (DR) consists of a dielectric material in a cylindrical form as shown in Fig. 10.70 which has a typical relative permittivity of ε_r = 30~100 and thus acts as a resonator due to the high dielectric constant.

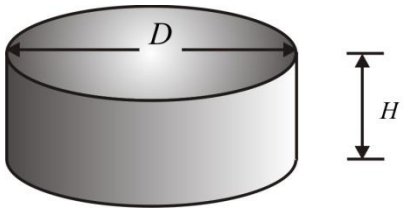


Figure 10.70 Structure of a dielectric resonator

The dielectric material used for DR generally has a low-loss and the dielectric resonator usually has a Q higher than 10^3. The size of dielectric resonator generally expands or shrinks according to changes in temperature, and because the resonant frequency of the dielectric resonator is related to the size of the dielectric resonator, this causes changes in the resonant frequency. Furthermore, the dielectric constant also changes with temperature, which also contributes to the change in the resonant frequency. Defining the thermal expansion coefficient and temperature coefficient of the dielectric constant as α_L and τ_ε respectively, the temperature drift in resonant frequency τ_f becomes

$$\tau_f \approx -\frac{1}{2}\tau_\varepsilon - \alpha_L \tag{10.53}$$

The temperature coefficient of the dielectric constant and thermal expansion coefficient are dependent on the dielectric material constituting the dielectric resonator; and by making the temperature coefficient of the dielectric constant to compensate for the thermal expansion coefficient, the temperature-drift of the resonant frequency of the dielectric resonator can be minimized. As a result of recent studies of dielectric resonator materials, most commercially available dielectric resonator in today are designed to make the temperature-drift of the resonant frequency almost zero. Similar to other resonators, several resonant modes are possible in a dielectric resonator, and the fundamental mode with the lowest resonant frequency has the electric field distribution shown in Fig. 10.71.

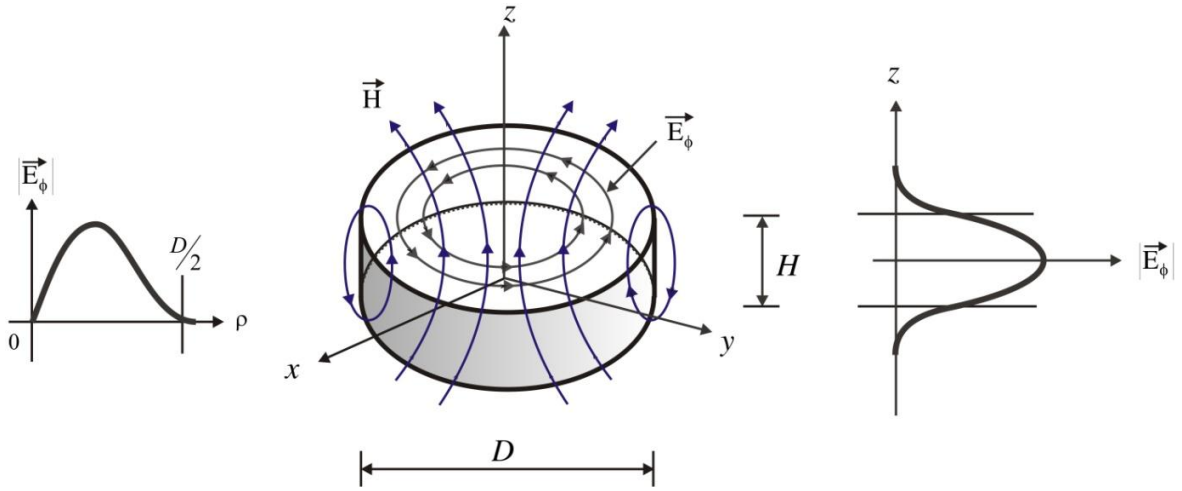


Figure 10.71 The electromagnetic field structure of a dielectric resonator

For the cylindrical $\rho\varphi z$ coordinate system as shown in Fig. 10.71, the direction of electric field appears in the φ-direction and is denoted as E_φ. The distribution of E_φ for z-axis shows a peak value at z=0, and rapidly decays going away from z=0 as shown in the figure. The distribution of E_φ for ρ-axis is 0 at ρ =0 and shows a peak value inside the dielectric resonator. The field E_φ also rapidly decays outside of the dielectric resonator. Thus, when the z direction is taken as the propagation direction, the field is said to be in a Transverse Electric (TE) mode because the electric field exists only in the vertical plane of the propagation direction. The distribution of the electric field E_φ can be represented by mode number which represents the standing wave form in each axis. The mode number in the ρ-axis is close to 1 and in the φ-axis is 0 since there is no standing wave. The mode number in the z axis is represented by δ since a complete standing wave is not established. Thus the resonant mode in Fig. 10.71is called as $TE_{10\,\delta}$ mode.

On the other hand, the shape of the magnetic field mainly occurs as passing through the dielectric resonator as shown in Fig. 10.71, which is generated by the time varying electric field E_φ according to Maxwell's equations. Note that the electric field inside the dielectric resonator is small and can be approximated as 0 as $\varepsilon_r \to \infty$ according to Maxwell's equations; otherwise infinite magnetic field occurs, which is not practically possible. Consider the case where the external magnetic field penetrates through the dielectric resonator as shown in the figure. The electric field E_φ is then generated according to Faraday's law of electromagnetism. The induced electric field E_φ again generates a magnetic field which occurs in a direction as to cancel the incident magnetic field. Since the dielectric resonator is not a magnetic material, the relative permeability can be considered to be 1, and finite electric field E_φ is induced. Then, the magnetic field generated by the finite induced electric field E_φ becomes ∞ due to $\varepsilon_r \to \infty$ as the generated magnetic field is proportional to the relative permittivity ε_r, which is practically not acceptable. As a result, the magnetic field inside the dielectric resonator is therefore close to 0. Otherwise, a small magnetic field can cause an infinite magnetic field in the opposite direction. This phenomenon of the electro-magnetic field in the dielectric resonator is similar to that of eddy current generated in a conductor in electromagnetism. Therefore, the magnetic field incident perpendicularly to the surface will almost be zero.

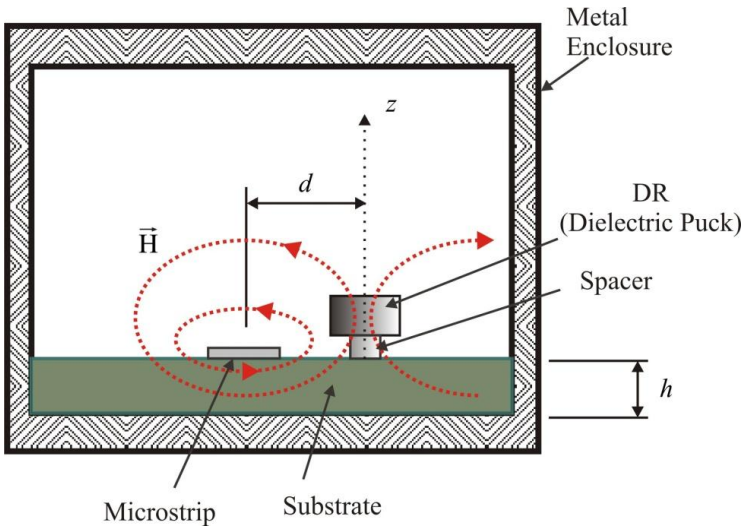
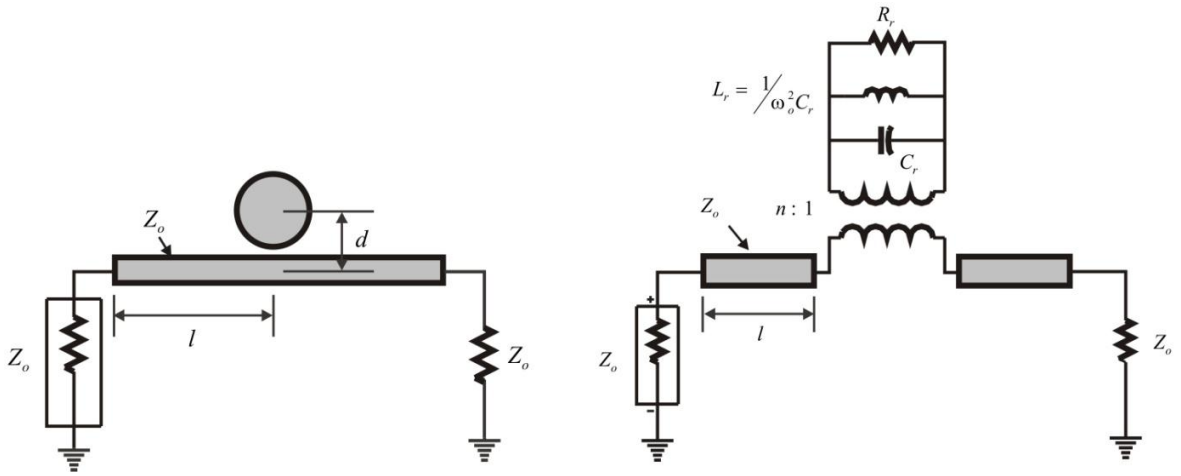
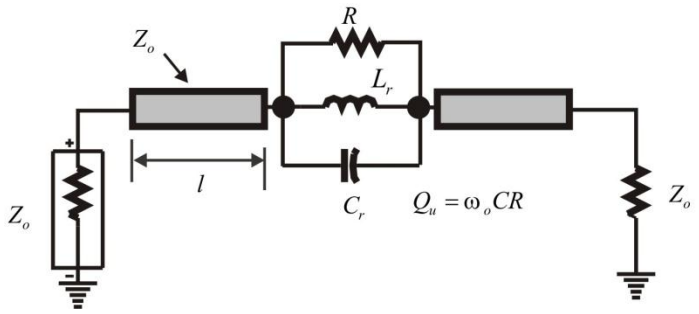


Figure 10.72 Coupling dielectric resonator to microstrip

Using the properties of the dielectric resonator previously described, the dielectric resonator is generally coupled to microstrip as shown in Fig. 10.72. The magnetic field from the microstrip is incident to the dielectric resonator as shown in Fig. 10.71 and the magnetic field penetrating the dielectric resonator becomes almost 0 at the resonant frequency of the dielectric resonator. In order to make the magnetic field lines easily penetrate the dielectric resonator vertically, the dielectric resonator must be positioned higher than the substrate on which the microstrip is placed. To effectively achieve this, a separate spacer is inserted beneath the dielectric resonator as shown in Fig. 10.72 which makes the possible magnetic field lines vertically penetrate the dielectric resonator. The magnetic field corresponds to the microstrip current; and since the magnetic field at the resonant frequency of the dielectric resonator is 0, the microstrip current will be zero. As a result, the microstrip will be open-circuited at the reference line where the microstrip is coupled with the dielectric resonator.

The circuit shown in Fig. 10.73(a) represent the dielectric resonator coupled to a microstrip, and its equivalent circuit can be represented as shown in Fig. 10.73 (b).





(c)

Figure 10.73 (a) Dielectric resonator circuit, (b) equivalent circuit, and (c) simplified equivalent circuit

When the distance *d* in Fig. 10.73(a) is small, the coupling between the dielectric resonator and the microstrip becomes tight, and the magnetic field of the microstrip is significantly affected by the dielectric resonator. On the other hand, when the distance is large, the coupling between the dielectric resonator and the microstrip becomes loose, and the effect of the dielectric resonator almost vanishes. Notably, the point where the magnetic field is 0 represents the length *l* where the microstrip is strongly coupled to the dielectric resonator in Fig. 10.73(a) and since the magnetic field is 0, the current also drops to 0 and the microstrip line is thus open-circuited at the length *l*.

The circuit in Fig. 10.73(a) is represented by the equivalent circuit shown in Fig. 10.73(b). Here, the transformer *n* represents the degree of coupling between the dielectric resonator and the microstrip, which is a function of *d* and the parallel resonant circuit L_r–C_r–R_r represents the dielectric resonator. The circuit in Fig. 10.73(b) can be transformed into the circuit in Fig. 10.73(c). The impedance seen from the transformer port connected to the microstrip line is a parallel resonant circuit and the circuit in Fig. 10.73(c) can be obtained. It must be noted that the resonance frequency of the circuit in Fig. 10.73(c) is the same as that in Fig. 10.73(b). However, the values of *R*, *L*, and C differ from those of R_r, L_r, and C_r. The value of resistor *R* reflects the degree of coupling between the dielectric resonator and the microstrip which is a function of *d*.

Setting $l = 0$ in the circuit of Fig. 10.73(c), the frequency response of the reflection coefficient seen from the input port can be plotted as shown in Fig. 10.74(a) with *d* as a parameter. The dielectric resonator has negligible effect on the microstrip line for frequencies outside the resonant frequency; consequently, the impedance seen from the port is close to Z_o=50 ohm and appears at the origin of the Smith chart. On the other hand, the impedance seen from the input port, at the resonant frequency, becomes $Z_o + R$ and this is represented by point A on the Smith chart in Fig. 10. 74(a). Furthermore, this point depends on the coupling between the microstrip and the dielectric resonator; when the coupling is very tight $R \rightarrow \infty$, the impedance appears at a point in ∞ of the Smith chart. Therefore, when the coupling is very tight, the approximately open impedance at the input port appears at the resonant frequency.

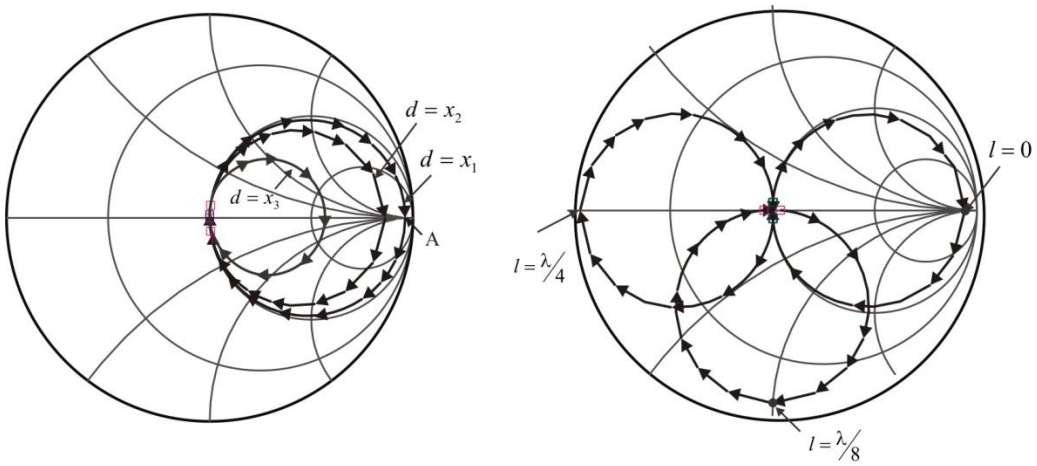


Figure 10.74 (a) Variation of S-parameter (l = 0) with respect to d and (b) Variation of S-parameters with respect to l

For the tightly coupled dielectric resonator, i.e. $d = x_1$, Fig. 10.74(b) shows the impedance locus seen from the port when the length of the microstrip line, l is varied. The input reflection coefficient Γ_{in} at the resonant frequency of the dielectric resonator is obtained by rotating $\Gamma(\omega_o)$ for l=0 in a clockwise direction by $2\theta_o(l)$.

$$\Gamma_{in} = \Gamma(\omega_o)e^{-2j\theta_o} \tag{10.54}$$

Here, $\theta_o(l)$ is the electrical length of the microstrip length l at the resonant frequency. Notably, any reactance around the unit circle of Smith chart can be implemented by varying the length l. Furthermore, such reactance appears only near the resonant frequency of the dielectric resonator and the impedance rapidly approaches Z_o as slightly away from the resonant frequency. This point is important in oscillator design. To emphasize this point, the circuit is re-drawn in Fig. 10.75(a) where the dielectric resonator is placed at a distance θ away from the port and the impedance locus of the circuit in Fig. 10.75(a) seen from the port is shown in the Smith chart in Fig. 10.75(b). In the circuit configuration of Fig. 10.75(a), the impedance seen from the port behaves as the open-circuited transmission line at θ near the resonant frequency as shown in Fig. 10.75(b), and the impedance becomes Z_o at other frequencies as the port is directly connected to the termination Z_o. Using this property, oscillation condition can be satisfied only at the resonant frequency. At other frequencies, the oscillator circuit is generally stabilized because the impedance seen from the port is close to Z_o and oscillation condition is not satisfied except at the resonant frequency. As a result, the undesired oscillation condition at other frequencies can be easily avoided.

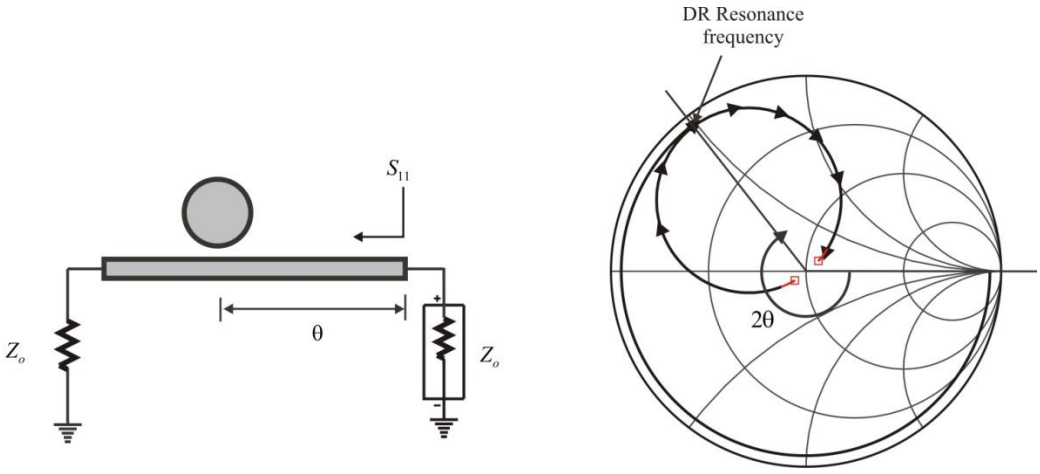


Figure 10.75 (a) A circuit of the DR coupled to microstrip and (b) its impedance locus seen from the port with frequency.

10.6.2 Extraction of the Equivalent Circuit of a DR Coupled to a Microstrip

In this chapter, we look at the method of extracting the values of the equivalent circuit for a dielectric resonator coupled to a microstrip. Denoting the impedance of the parallel resonant circuit in the circuit of Fig. 10.73(c) as Z_p, the reflection coefficient seen at port 1 becomes,

$$S_{11} = \frac{Z_p + Z_o - Z_o}{Z_p + Z_o + Z_o} e^{-2j\theta} = \frac{Z_p}{Z_p + 2Z_o} e^{-2j\theta} \tag{10.55}$$

where

$$Z_p = \frac{1}{\frac{1}{R} + j\omega C + \frac{1}{j\omega L}} \cong \frac{R}{1 + 2jQ_u \frac{\Delta\omega}{\omega_o}} \tag{10.56a}$$

$$f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{\omega_O}{2\pi} \tag{10.56b}$$

$$Q_u = \omega_o CR \tag{10.56c}$$

Here, Q_u is the intrinsic Q of the dielectric resonator and is known as unloaded Q. Substituting Z_p into equation (10.55) and re-arranging,

$$S_{11} = \frac{\beta}{1+\beta+2jQ_u\dfrac{\Delta\omega}{\omega_o}}e^{-2j\theta} = \frac{\dfrac{\beta}{1+\beta}}{1+2jQ_L\dfrac{\Delta\omega}{\omega_o}}e^{-2j\theta} \tag{10.57a}$$

$$\beta = \frac{R}{2Z_o} \tag{10.57b}$$

$$Q_L = \frac{Q_u}{1+\beta} \tag{10.57c}$$

Thus, the frequency response of $|S_{11}|$ when plotted is as shown in Fig. 10.76.

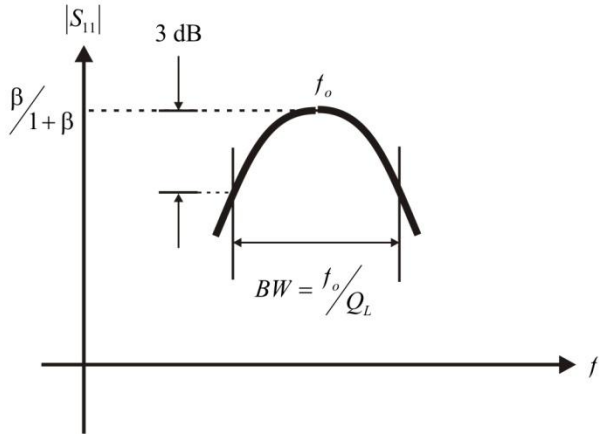


Figure 10.76 The frequency response of the dielectric resonator coupled to the microstrip circuit.

From equation (10.57a), it can be found that the frequency corresponding to the peak value of $|S_{11}|$ becomes the resonant frequency. Since the peak value at the resonant frequency is $\beta/(1+\beta)$, β can be obtained from the measured peak value. As a result, the value of R can be obtained using equation (10.57b). Furthermore, when the 3-dB bandwidth is measured as shown in Fig. 10.76, Q_L can be found from

$$Q_L = \frac{f_o}{BW} \tag{10.58}$$

Thus, the unloaded Q, Q_u can be determined by substituting the obtained values of β and Q_L into equation (10.57c), from which the value of C can be determined using equation (10.56c). Furthermore, the value of L can be obtained from the resonant frequency and C using equation (10.56b). Thus all the parameter values of the equivalent circuit can be determined using the frequency response of $|S_{11}|$.

■ Example 10.14

Figure 10E.26 shows the frequency response of $|S_{11}|$ for a dielectric resonator coupled to a microstrip circuit. In Fig. 10E.26, f_o = 10 GHz, $|S_{11}|_{max}$ =–7.06 dB, and BW = 90 MHz. Calculate the values of the equivalent circuit of the microstrip circuit coupled to the dielectric resonator in Fig. 10.73(c).

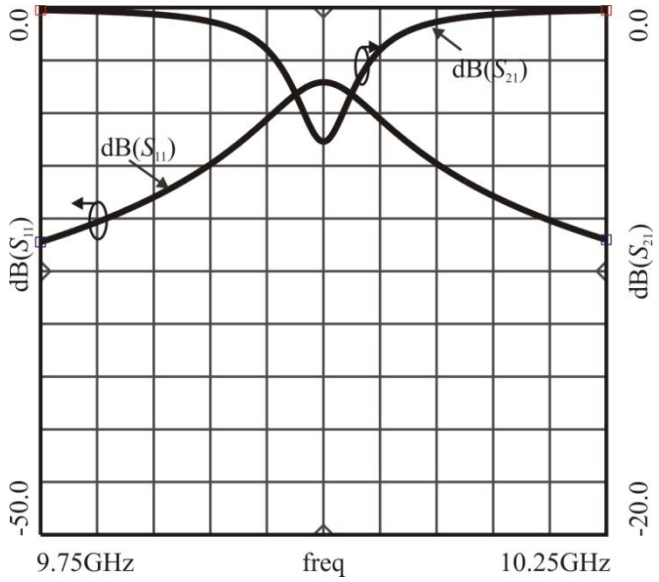


Figure 10E.26 The frequency response of the dielectric resonator coupled to the microstrip circuit

Solution

From $|S_{11}|_{max}$ =–7.06 dB, β can be obtained as follows:

$$\frac{\beta}{1+\beta} = \left|S_{11}\right|_{\max} = 10^{-7.06/20} = 0.444,$$

$$\beta = \frac{0.444}{1-0.444} = 0.799 = \frac{R}{2Z_o}$$

From this, the value of R can be obtained as

$$R = 80\Omega$$

Furthermore, from BW=90, resonant frequency, f_o = 10 GHz, Q_L and Q_u can be obtained as follows:

$$Q_L = \frac{f_o}{BW} = 111 = \frac{Q_u}{1+\beta} = 199.8 = \omega_o CR$$

Thus,

$$C = \frac{199.8}{2\pi f_o R} = 39.73 \text{ pF}$$

The value of L is also obtained from ω_o as follows:

$$L = \frac{1}{\omega_o^2 C} = \frac{1}{(2\pi f_o)^2 C} = 6.38 \text{ pH}$$

Therefore, the values of the components in the equivalent circuit yielding the given frequency response are as follows:

$$R = 80\Omega, \; C = 39.73 \text{ pF}, \; L = 6.38 \text{ pH}$$

■

The method of Example 10.14 uses S-parameters to extract the equivalent circuit of the dielectric resonator coupled to microstrip. The S-parameters can be obtained from measurement or from the 3D simulation of the dielectric resonator coupled to a microstrip. In the following example, we will show the extraction of the equivalent circuit parameters using a program developed by TransTech.

■ Example 10.15

Download the computing program for the parameters of dielectric resonators from TransTech website, and use it to compute the values of the equivalent circuit parameters of the dielectric resonator coupled to a microstrip. The selected dielectric resonator is Murata's DRD107UC048, which has the parameters ε_r = 37.7 Q_u = 6800 at the frequency of 7 GHz. This resonator has a diameter of D = 10.75 mm and heigth H_D = 4.77 mm and is mounted on a spacer having a diameter D_s = 8.001 mm, thickness t_s = 1.016 mm and dielectric constant ε_r = 4.5. The selected substrate is RT/Durooid 4350, whose dielectric constant is ε_r = 3.66, thickness H = 30 mil. After adjusting the resonant frequency to 5.3 GHz, determine the equivalent circuit parameters of the dielectric resonator placed away from a 50 ohm microstrip by d=6.5 mm. The distance d is defined as shown in Fig. 10.73 (a).

Solution

Figure 10E.27 is the initial setup window after installation. Set up the parameters as shown in Fig. 10E.27, and by selecting Thin Substrate, the window shown in Fig. 10E.28 is displayed. Notably, the diameter and height of the cylindrical conductor box surrounding the dielectric resonator is set to 30.86 mm and 13.87 mm, respectively. Furthermore, the height of the tuning screw for the tuning of the resonant frequency is initially set to 0. By entering the dimensions given in the problem of Fig. 10E.28 or clicking the Auto Tune utility, Fig. 10E.28 will be displayed. The length of the tuning screw obtained can be seen to be 4.75 mm.

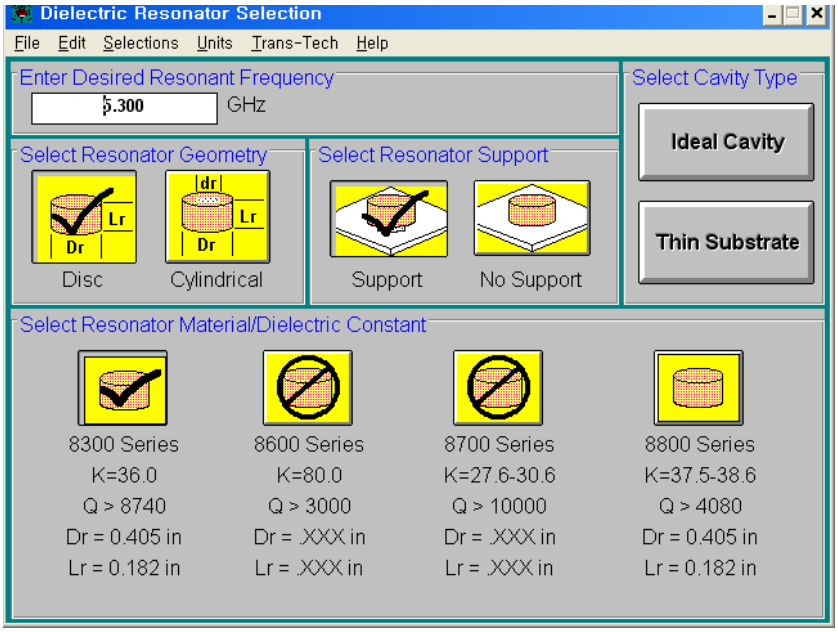


Figure 10E.27 Initial Setup Window of the Dielectric Resonator

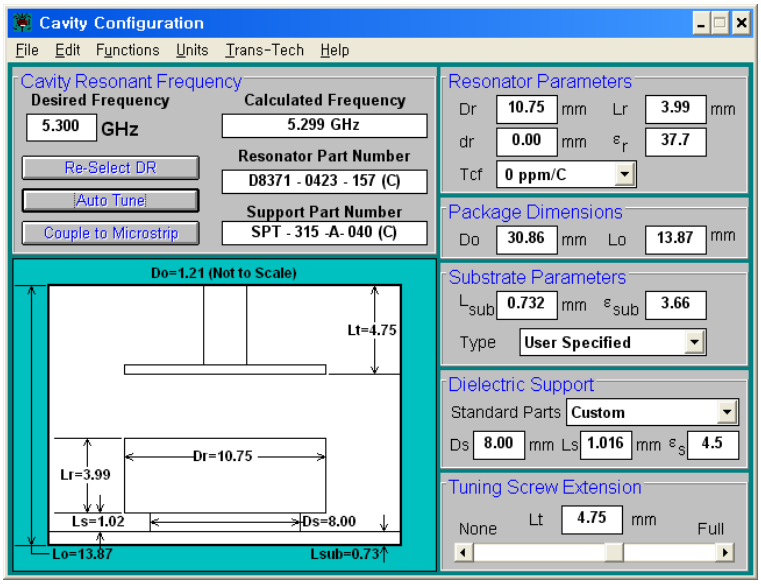


Figure 10E.28 Variation of the resonance frequency according to changes in tuning screw height

Selecting **Couple DR to microstrip** from the Function menu bar of Fig. 10E.28 will display a new window as shown in Fig. 10E.29. Select aluminum as the material for the conductor box and set the distance between the dielectric resonator and the microstrip to D = 6.5 mm. The values of the equivalent circuit components will be displayed as shown Fig. 10E.29

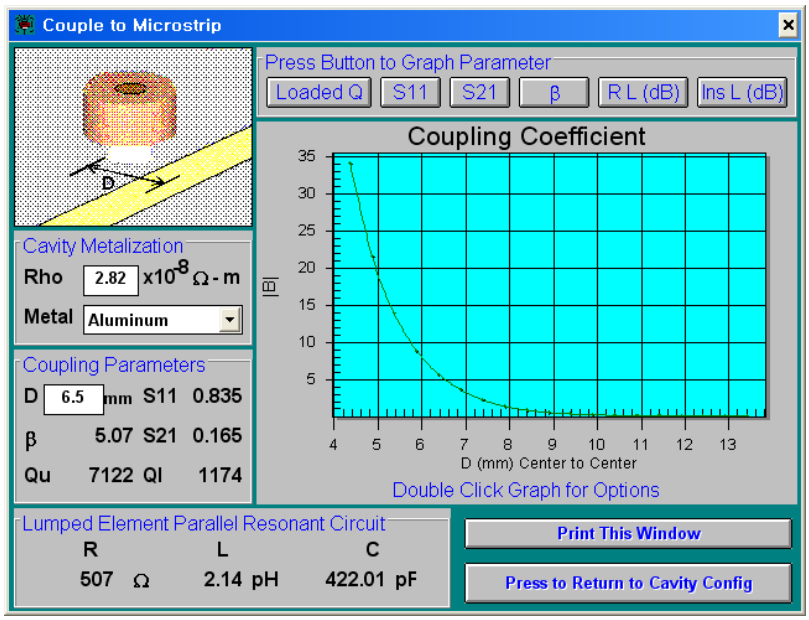


Figure 10E.29 Equivalent circuit values for the selected coupling distances

■

10.6.3 Design of Dielectric Resonator Oscillator (DRO)

We saw in the preceding sections that, a microstrip oscillator can be designed by replacing the capacitors and inductors of the series feedback oscillator prototype by open or short-circuited microstrip lines. There are several ways of designing DROs (dielectric resonator oscillators) but the simplest method is to design a DRO by replacing one of open or short-circuited microstrip lines by a dielectric resonator coupled to microstrip circuit as previously described. Another method is to use the dielectric resonator as a feedback resonator circuit. This chapter will discuss these two design methods.

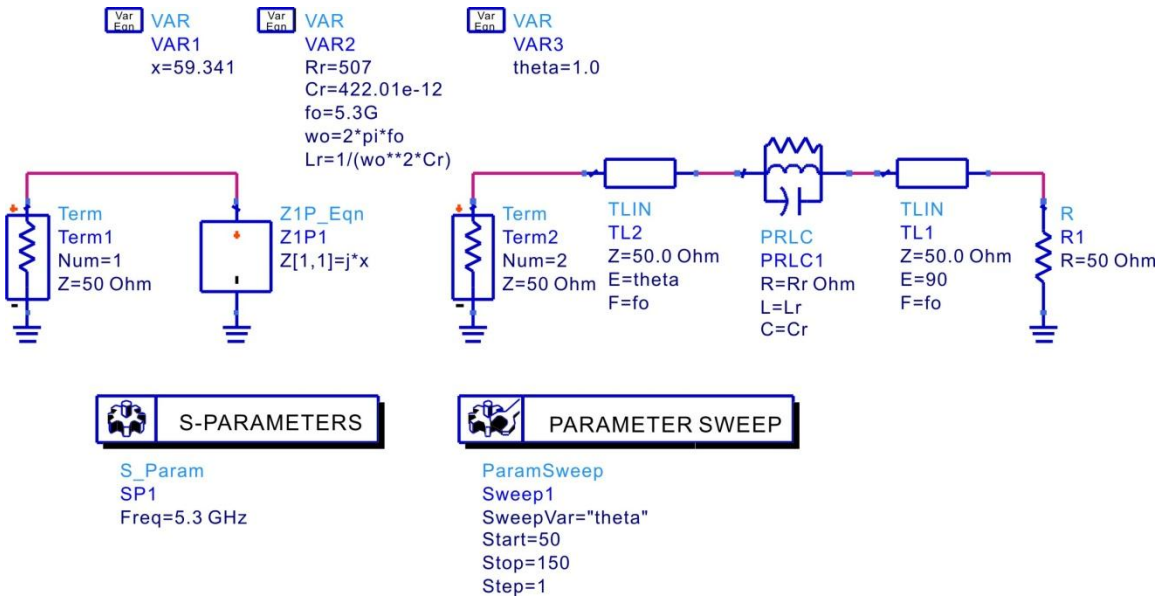
10.6.3.1 DRO Design Based on Replacement of LC

We look at how to design of a DRO using the design of the series feedback oscillator, shown in Example 10.13, at 5.3 GHz. Set the gain back-off factor g = 10 and compute x, y and Z_L at a frequency of 5.3 GHz in the same way as shown in Example 10.13. Then, the values of x, y and Z_L can be obtained as

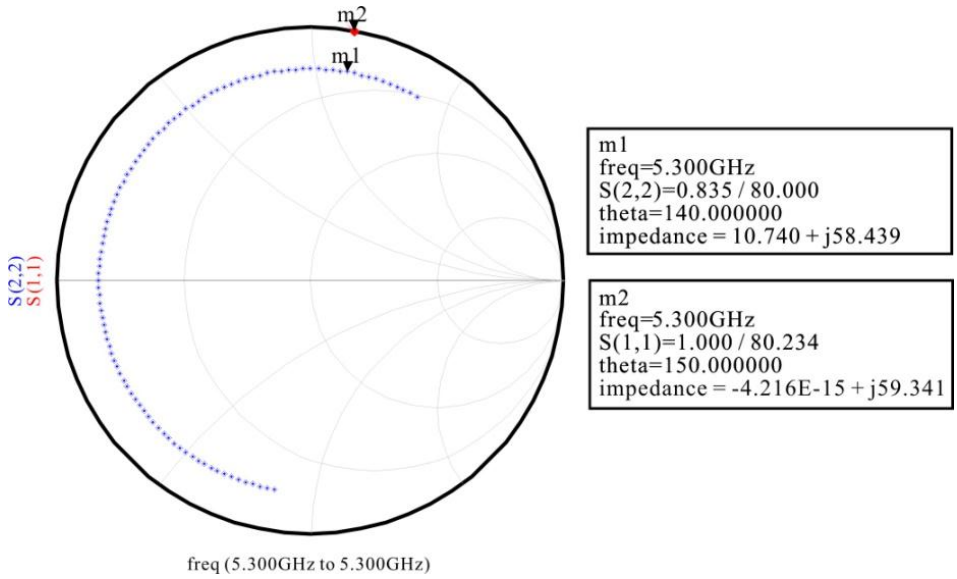
x	y	ZL
59.341	-15.507	36.171+j5.689

Using these values, the microstrip oscillator can be designed by following the design procedure of the microstrip oscillator shown in chapter 10.5. That is, x can be implemented using a short-circuited microstrip stub whereas y can be implemented using an open-circuited microstrip stub. Note that the gate is grounded at DC because x is implemented using the short-circuited microstrip

stub. Here, to add a circuit for self DC bias, resistor R_S in series with RFC are added to the source terminal and the value of the source resistor R_S can be set to satisfy a drain voltage and current of 2V and10mA, respectively. Thus, the microstrip oscillator can be designed by implementing the appropriate load circuit.



(a)



(b)

Figure 10.77 (a) Implementation of *x* using dielectric resonator coupled to microstrip circuit and (b) simulation results

The DRO can be configured by replacing either *x* or *y* of the microstrip oscillator with a microstrip line coupled to a dielectric resonator circuit shown in Fig.10.73. When *x* is replaced

using the circuit of the dielectric resonator coupled to microstrip, the gate terminal becomes connected to resistance R = 50 ohm at DC. However, since DC current does not flow through the gate terminal, the DC operating point is not affected by the resistor 50 ohm. On the other hand, replacing *y* with the dielectric resonator coupled to microstrip will change the DC operating point. It is possible to maintain the DC operating point by adding some extra circuits, but the procedure is somewhat complex. Therefore, it is more convenient to replace the inductor on the gate side with the dielectric resonator coupled to microstrip.

The next problem is, the dielectric resonator coupled to microstrip circuit cannot be considered as pure reactance but one that has loss. It is difficult to determine the values of the series feedback oscillator prototype taking these losses into consideration. However, assuming that the impedance seen into the active part is sufficiently high enough to compensate for this loss in the dielectric resonator coupled to microstrip circuit, it is possible to design an approximate dielectric resonator oscillator by ignoring this loss.

Figure 10.77(a) is a simulation circuit for implementing *x* connected to the gate terminal as a dielectric resonator coupled to microstrip circuit. The results obtained from Example 10.15 are used for the parameters of the dielectric resonator coupled to microstrip circuit and, for the purpose of simplified calculation; an ideal transmission line was used instead of the microstrip. However, the design using this method is essentially the same as when using a microstrip for the design. To determine the position of the dielectric resonator in the microstrip, the length of the transmission line is varied with the frequency fixed to the resonant frequency of the dielectric resonator. This circuit is on the right side of Fig. 77(a). The given value of *x* is implemented using 1-port equation component as shown on the left side of Fig. 10.77(a). The desired position is **theta** which yields a reactance equal to the given value of *x*.

The simulation results are shown in Fig. 10.77(b). The locus with respect to **theta** is a circle with constant reflection coefficient due to the losses of the dielectric resonator coupled to microstrip circuit. From Fig. 10.73 (b), the electrical length giving the desired value of *x* for the dielectric resonator coupled to microstrip circuit can be seen to be approximately 140°. If the negative resistance of the active part is greater than the resistance occurring in the dielectric resonator coupled to microstrip circuit, oscillation will occur approximately at the resonant frequency. However, given that the negative resistance of the active part is not greater, then the gain back-off factor *g* is increased and new values of *x*, *y* and Z_L are calculated and the design procedure may be repeated.

OscTest is inserted as shown in Fig. 10.78 to investigate whether the designed dielectric resonator oscillator oscillates near 5.3 GHz. Furthermore, for the sake of comparison, the oscillation conditions of an oscillator without the dielectric resonator are also investigated.

Figure 10.79 shows the simulation results. It must be noted that the frequency satisfying the oscillation condition slightly changes according to the value of the reference impedance of **OscTest**. Refer to the Appendix E for details. The reference impedance here is set to 50 ohm. From Fig. 10.79, the DRO can be seen to satisfy the oscillation condition near 5.3 GHz. In addition, you can see that the reference oscillator also satisfies the oscillation condition at 5.3 GHz. As the *Q* of the dielectric resonator oscillator is high, it can be seen to satisfy the oscillation condition in a very narrow band. On the other hand, the oscillation condition of the reference oscillator changes slowly with the frequency.

The disadvantage of such a design is that it may not take full advantage of the high *Q* of the dielectric resonator. Note that the loss of the dielectric resonator coupled to microstrip circuit is small for a large value of β according to equation (10.57a). Such a large value of β lowers the value of Q_L in equation (10.57c). Consequently, the phase noise performance of DRO which is related to

Q_L becomes poorer. Thus, the design to take advantage of the high Q of a dielectric resonator requires that, the losses of the dielectric resonator coupled to microstrip circuit be taken into account.

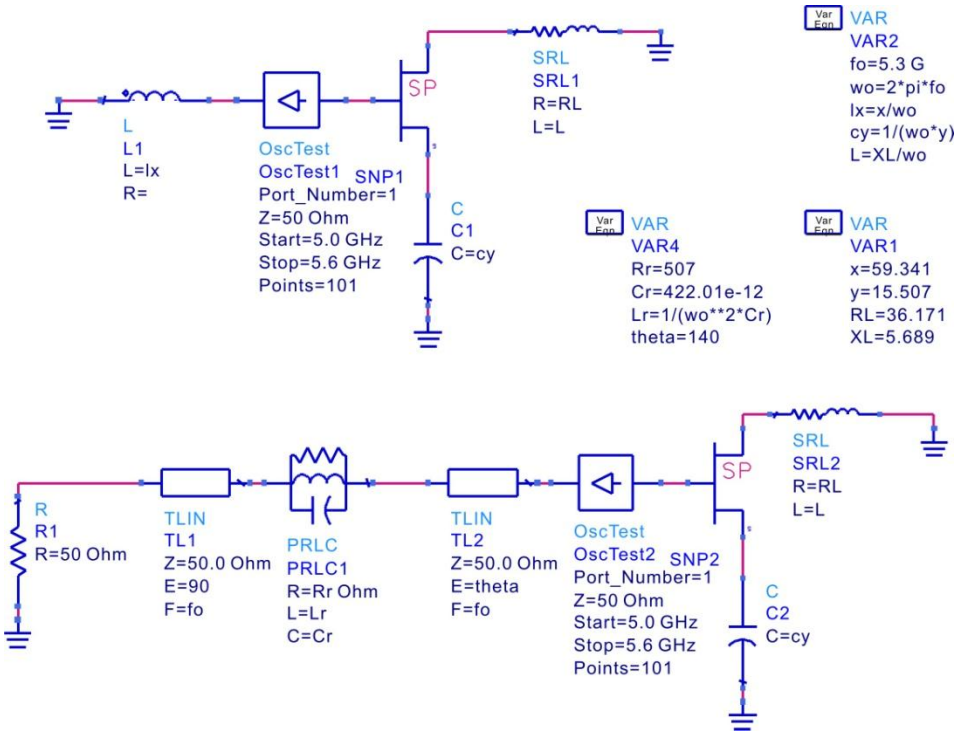


Figure 10.78 Series feedback oscillator prototype and Dielectric resonator oscillator circuit

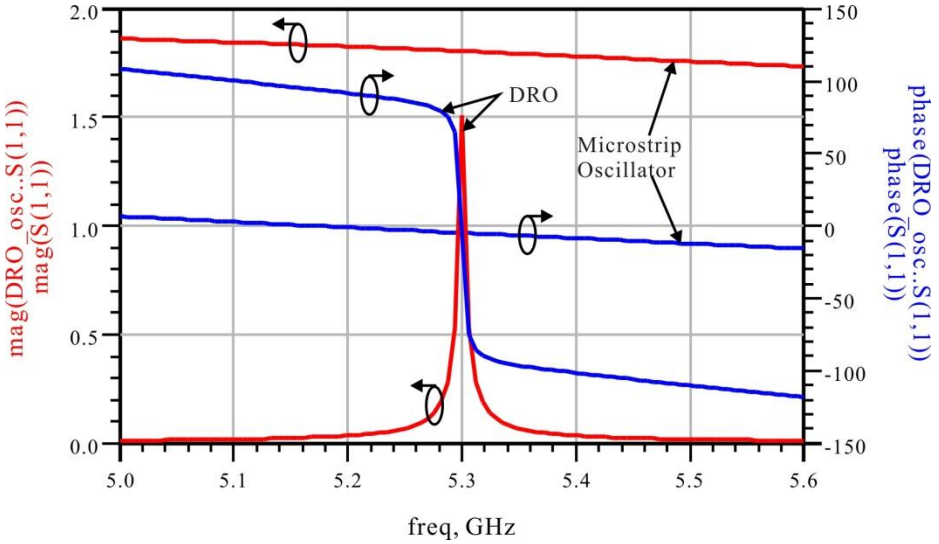


Figure 10.79 The oscillation conditions of the DRO circuit and series feedback oscillator prototype

10.6.3.2 Dielectric Resonator Oscillator Design Using Feedback

Another way of designing a DRO is as shown in the oscillator circuit configuration of Fig. 10.80. The dielectric resonator here is used in place of the resonator of Fig. 10.80. Here, the amplifier provides a sufficient loop gain, the oscillation frequency is adjusted using the phase shifter, and the output power is obtained by coupling a part of the oscillation power in the loop.

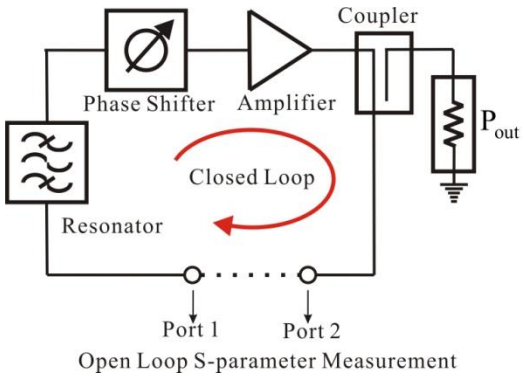


Figure 10.80 Dielectric resonator oscillator circuit

The open-loop gain $L(\omega)$ can be expressed using 2-port S-parameters of the cascade chains of the resonator, phase shifter, and amplifier using equation (10.18). Generally, each component in Fig. 10.80 is usually designed to have a small reflection in order to avoid a mismatch between components connected in cascade. Thus, S_{11} and S_{22} of the open-loop gain S-parameters can be assumed to be small. Furthermore, the reverse gain S_{12} is small due to the properties of the amplifier. Assuming S_{11}, S_{22} and S_{12} are small, the following equation can be derived.

$$L(\omega) \cong S_{21} \tag{10.59}$$

Thus, from equation (10.59), the oscillation condition can be re-written as

$$\mathrm{dB}(S_{21}) \geq 0 \tag{10.60a}$$

$$\mathrm{phase}(S_{21}) = 0 \tag{10.60b}$$

The open loop gain method previously discussed provides an easy design of an oscillator. To design an oscillator based on the open loop gain method, by connecting the amplifier, phase shifter and the resonator sequentially and the 2-port S-parameters of the cascade chains is measured in an open loop state. Then, when the two equations of (10.60) are satisfied at the oscillation frequency, the oscillator can simply be formed at the desired frequency by closing the open loop. In addition, the oscillation frequency can be adjusted using the phase shifter. Since the oscillation frequency occurs where the phase of S_{21} is 0, the phase of the open-loop gain can be adjusted using the phase shifter, which results in the change of the oscillation frequency. Typically, the amplifiers and phase shifters in Fig. 10.80 have broadband characteristics and only the resonator has narrowband characteristics. Thus, the frequency response of the open-loop gain appears similar to that of the resonator as shown in Fig. 10.81.

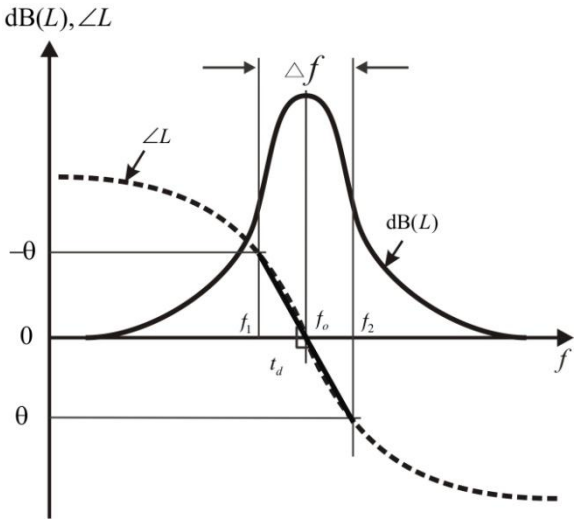


Figure 10.81 The frequency response of the open loop gain

Given that a phase shifter has a maximum phase shift of $\pm\theta$, due to this phase shifter, it can be seen that the oscillation frequency is found to be tuned to the corresponding frequencies f_1 and f_2 from Fig. 10.81. Thus, an electrical frequency tuning range of $\Delta f = f_2 - f_1$ is obtained by adjusting the phase shifter. The slope of the phase of the open loop gain at the center frequency f_o becomes the group delay of the loop gain which is defined by the following equation:

$$t_g = -\left.\frac{\partial\phi}{\partial\omega}\right|_{\omega=\omega_o} \tag{10.61}$$

Using this, the electrical frequency tuning range Δf becomes

$$\Delta f \cong \frac{1}{180}\frac{\theta}{t_g}, \tag{10.62}$$

Here, θ is expressed in degrees. Thus, the higher the group-delay, the narrower the electrical frequency tuning range.

The phase noise $S(f_m)$ based on Lesson's empirical formula can be expressed as:

$$S(f_m) = -10\log\left\{\frac{1}{2}\frac{FkT}{P}\left[1+\left(\frac{1}{f_m}\frac{f_o}{2Q}\right)^2\right]\right\} \tag{10.63}$$

Here, f_m represents the offset frequency, P and F represent the oscillation output power and noise figure of the amplifier respectively. The Q in equation (10.63) becomes the Q_L of the open loop gain, and Q_L is expressed in terms of the group delay as,

$$Q_L = \pi f_o t_g \tag{10.64}$$

Therefore, the phase noise can be seen to improve as the group delay increases. Phase noise improvement as a result of group delay improvement is quite obvious from equation (10.63).

Suppose that a phase noise of S_1 (dBc/Hz) is obtained when the oscillator of Fig. 10.80 is configured using a resonator having a group delay of t_{g1}. Assuming the group delay of the resonator is improved to t_{g2}, and an oscillator of the same structure is fabricated using the improved resonator. The resulting electrical frequency tuning range will be reduced by $t_{g2}/\ t_{g1}$ while the phase noise of the newly designed oscillator S_2 (dBc/Hz) will be improved by

$$S_2 = S_1 - 20\log\frac{t_{g2}}{t_{g1}} \tag{10.65}$$

Thus, the phase noise can be systematically improved using the open loop method. In conclusion, from equations (10.62) and (10.63), the electrical frequency tuning range and the phase noise are found to have a trade-off relationship and the group delay of the open-loop gain is found to be a key parameter of this trade-off relation.

From the design point of view, the phase shifter, amplifier, and resonator are independently designed in advance and the designed components are connected in cascade to form the oscillator. Denoting the S-parameters of the phase shifter, amplifier, and resonator as S_φ, S_A, and S_R, respectively, the open-loop gain S_{21} can be expressed as,

$$S_{21} = S_{R,21}S_{\phi,21}S_{A,21} \tag{10.66}$$

Therefore, in order to satisfy the oscillation conditions given by equation (10.60), the magnitude of S_{21} has to be set greater than 1 and the phase of S_{21} should satisfy

$$\phi = \phi\big|_{resonator} + \phi\big|_{amplifier} + \phi\big|_{shifter} = 0 \tag{10.67}$$

Typically, the sum of the phases of the amplifier, resonator and the phase shifter does not satisfy equation (10.67). In this case, the oscillator can be designed by adding a 50 ohm transmission line with the appropriate electrical length to satisfy equation (10.67). In addition, the group delay of the open-loop gain can be obtained by differentiating equation (10.67) with respect to frequency, and the sum of the group delays of each component becomes the group delay of the open loop gain. However, as the group delay of the resonator is the dominant, the group delay is determined by that of the resonator. Thus, the resonator must be designed to have the group delay that satisfies the design goal of the oscillator.

When the group delay of the loop gain is determined using the group delay of the resonator, the next task is to set the phase-shifter to satisfy the electrical frequency tuning range. To achieve this, the amount of phase-shift of the phase shifter is set to satisfy equation (10.62). Furthermore, the amplifier must be designed to have a gain sufficiently high enough to yield the open-loop gain greater than 0 dB. The phase of the open-loop gain does not generally satisfy equation (10.67) when the open loop is formed using the designed resonator, phase shifter, and amplifier. Thus, a 50-ohm transmission line of the appropriate electrical length should be inserted to satisfy equation (10.67) and finally the oscillator of desired frequency can be designed. This method is a useful and efficient method not only for theoretical design but also for experimental design of an oscillator.

Figure 10.82 shows a resonator configured using a dielectric resonator. The selected dielectric resonator is Murata's DRD107UC048, which at the frequency of 7 GHz has parameters ε_r = 37.7

and Q_u= 6800. The resonant frequency of the dielectric resonator can be adjusted from 4.96 to 5.40 GHz with a metal box enclosure. The substrate used is RT Duroid 4350 whose permittivity is ε_r = 3.66 having thickness H =30 mil. The spacer in Fig. 10.82 is composed of a ceramic material and has a thickness of 1.016 mm and relative permittivity ε_r = 4.5. The spacer helps the magnetic field from the microstrip pass through the dielectric resonator vertically, which helps to remove the parasitic resonances of the resonator appearing near the resonance frequency. The group delay and resonant frequency of the resonator are slightly affected by the spacer. The height of the spacer is the main parameter for these changes of the group delay and resonant frequency because the permittivity of the spacer is much lower compared to the permittivity of the dielectric resonator. The resonance frequency can be adjusted within a frequency range of 100 MHz using the tuning screw which is fixed on the ceiling of the metal box enclosure. The effect of tuning on the group delay is small and negligible. The structure in Fig. 10.82 was analyzed using Ansoft's HFSS^{TM} to obtain the desired resonant frequency of 5.3 GHz by adjusting the tuning screw. The detailed dimensions yielding the resonant frequency of 5.3 GHz are shown in the caption of Fig. 10.82.

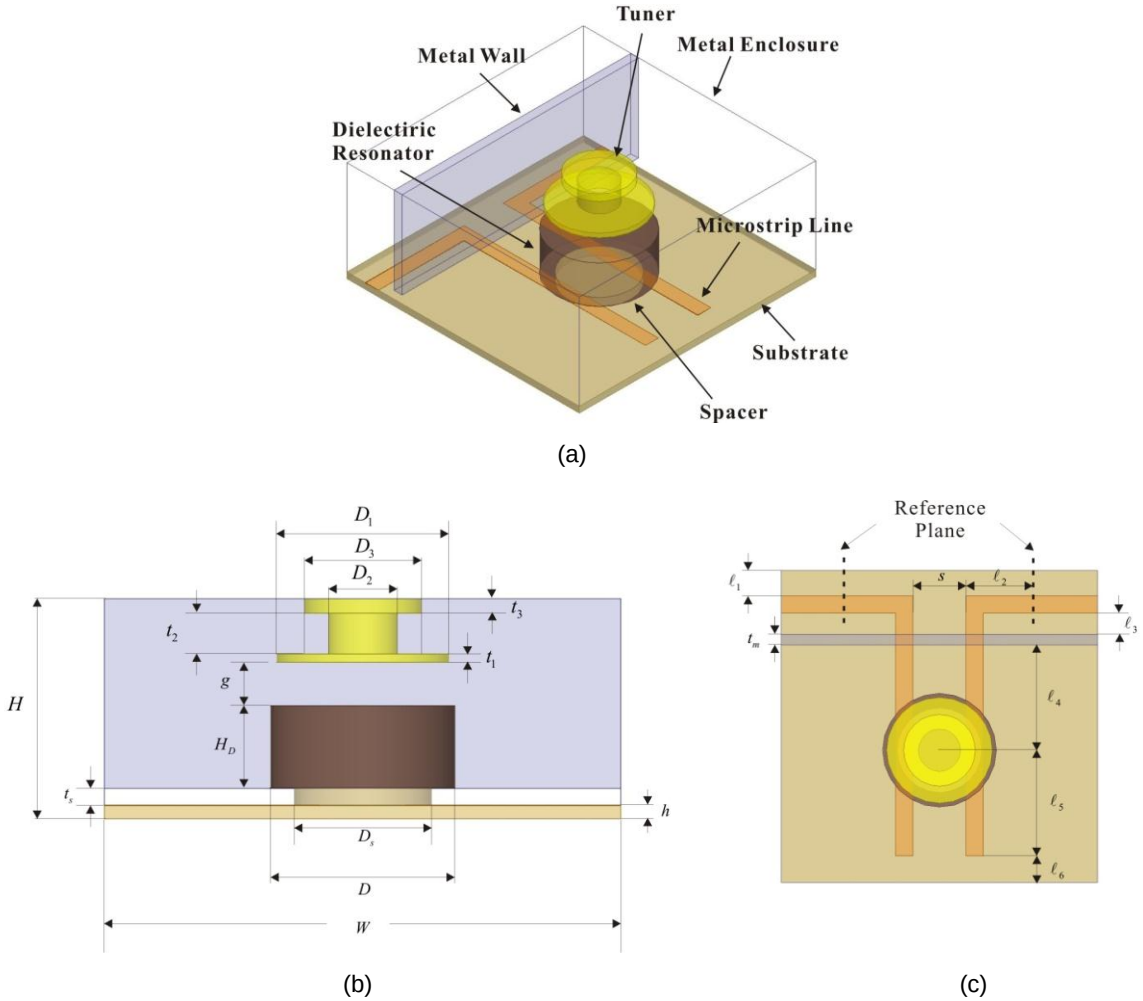


Figure 10.82 (a) Resonator structure, (b) front view; dimensions: W=30, H=12.762, h= 0.762, D_s=8.001, t_s=1.016, D=10.75, H_D=4.77, g=2.514, t_1=0.5, t_2=2.35, t_3=0.85, D_1=10, D_2=4, D_3=6.8, and (c) top view; Dimensions: l_1=2.36, l_2=6.5, l_3=2.0, l_4=10.0, l_6=2.5, d=5.6, w=1.64 (All units are in mm)

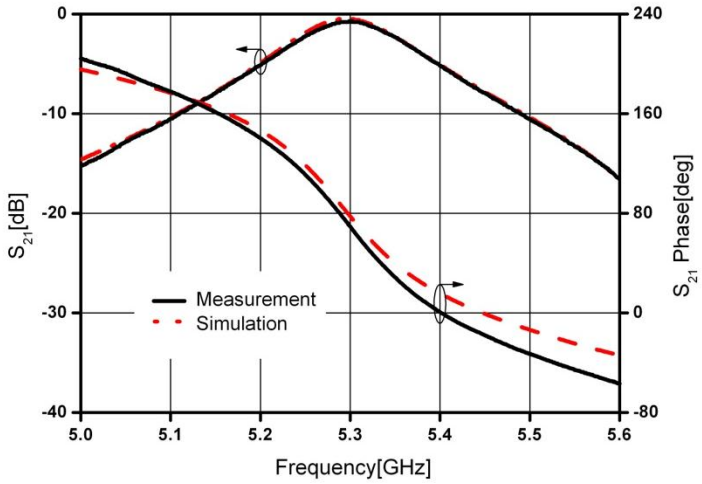


Figure 10.83 Measured and simulated S-parameters of the resonator

Figure 10.83 shows the simulated and measured S-parameters for the resonator shown in Fig. 10.82. The two results can be seen to agree very closely. The measured group delay can be derived using the slope of the phase against frequency in Fig. 10.83 and the value was measured to be 2.3 nsec as in the simulation. Using the group delay, the loaded Q, Q_L can be computed from equation (10.64) and the value is calculated to be 38.3. In addition, the electrical frequency tuning of about 84.5 MHz is estimated from equation (10.62) when the phase shifter with a phase shift of ± 35° is employed in the oscillator.

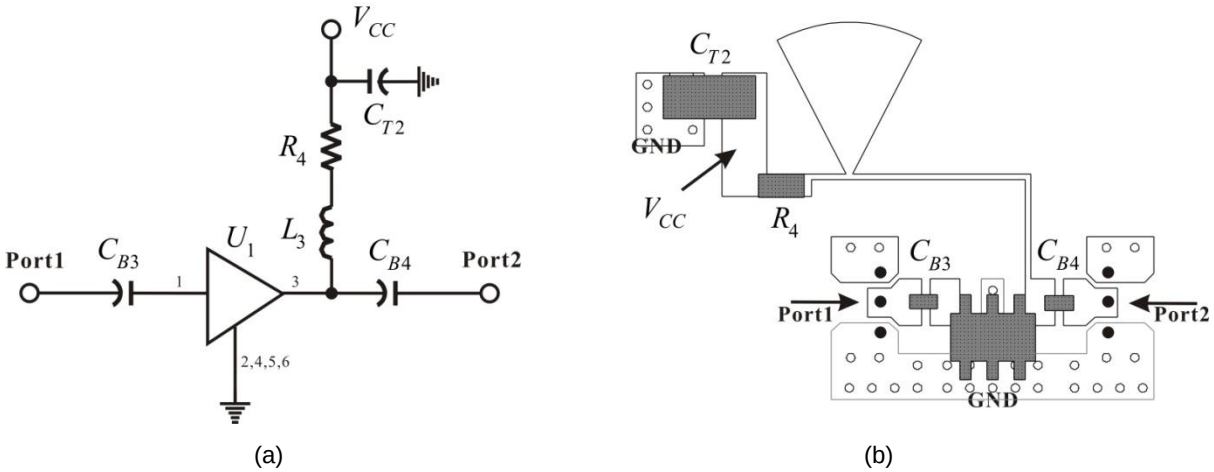


Figure 10.84 (a) Amplifier schematic U_1=HMC323, R_4=0, C_{T3}=0.33 uF, L_3 is a ¼ wavelength choke, C_{B3} and C_{B4} are 100 nF high frequency DC block capacitors and (b) amplifier Layout

The amplifier layout is shown in Fig. 10.84. Figure 10.84(a) represents the schematic and Fig. 10.84(b) shows the layout. The points marked with ● in Fig. 10.84(b) represent wafer probe contact pads which allow 2-port S-parameter measurement through on-wafer probing. From the datasheet, the selected amplifier HMC313 from Hittite shows an S_{21} magnitude and phase of 17 dB, –75° respectively for a DC bias of 5 V and DC current of 47 mA. All the chip DC block capacitors in Fig. 10.80(b) have a value of 100 nF, and the bypass capacitor C_{T2} is a 0.33 uF chip tantal capacitor.

The measured results slightly differs from the results provided in the datasheet due to the effect of the 50 ohm microstrip lines inserted for mounting the DC block capacitors and HMC313.

Figure 10.85 shows the measured results and datasheet values of S_{21}. The measured results can be seen to have a gain of 16.1 dB and a phase of approximately 52.5° within the frequency band of interest. The measured gain, S_{21} has a similar magnitude to the value from the datasheet, but the phase can be seen to show a significant difference. As described above, this is due to the effects of the 50 ohm microstrip line lengths inserted for mounting the DC block capacitors and HMC313. However, it can be seen that, the gain of the amplifier is sufficiently high to compensate the insertion losses of the resonator, phase shifter, and output coupler.

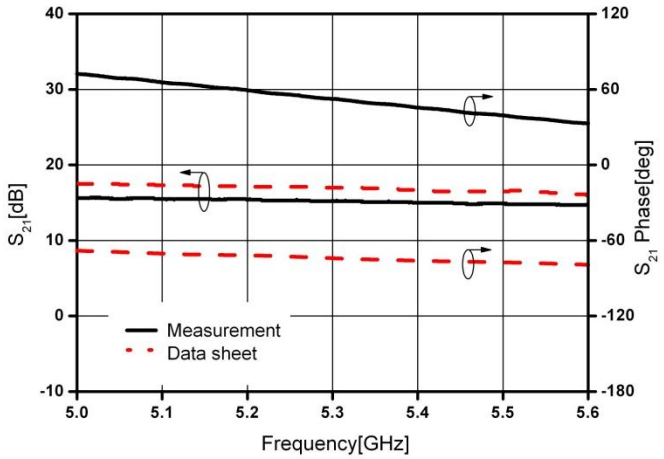


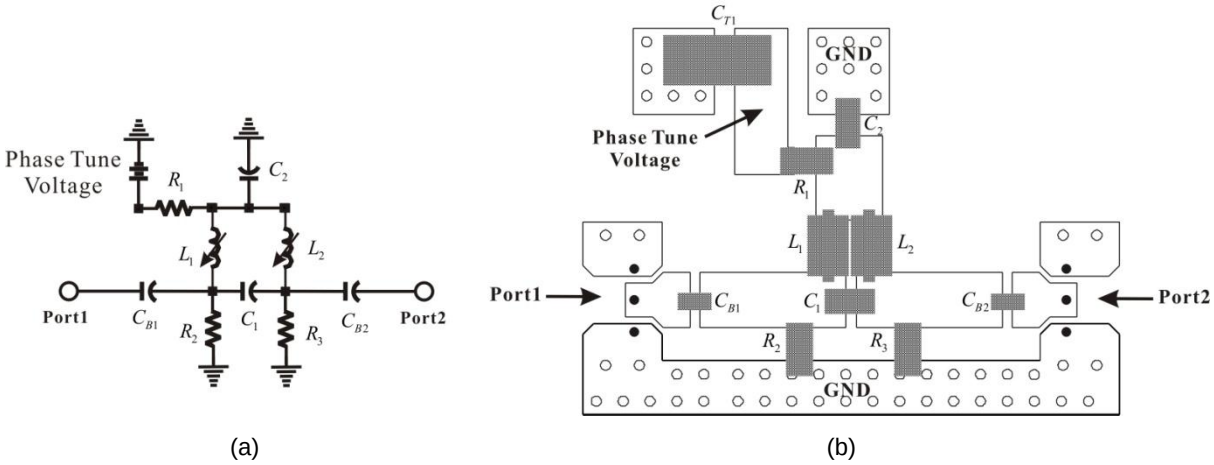
Figure 10.85 Comparison of the amplifier gains from datasheet and measurement

Figure 10.86(a) shows the phase shifter circuit. In Fig. 10.86(a), L_1 and L_2 are implemented using the identical varactor diodes, SMV1245 from Skyworks Inc. The diode SMV1245 is series resonant due to packaging inductance and the series resonant frequency is approximately 1.5 GHz. Therefore, when used near the oscillation frequency of 5.3 GHz, the varactor diode acts as a variable inductor. The two varactor diodes are biased by resistors R_1, R_2 and R_3. The reason for using the resistors in the DC bias is to remove the parasitic resonance phenomenon that occurs when using RF choke. Capacitors C_{B1} and C_{B2} are 100 nF high frequency DC block capacitors. Thus, when the DC block and the DC bias resistor are removed, this circuit becomes a traditional all pass filter and the capacitors C_1 and C_2 can determined from [16]

$$C_1 = \frac{1}{2\omega_o Z_o} \tag{10.68a}$$

$$C_2 = \frac{1}{\omega_o Z_o} \tag{10.68b}$$

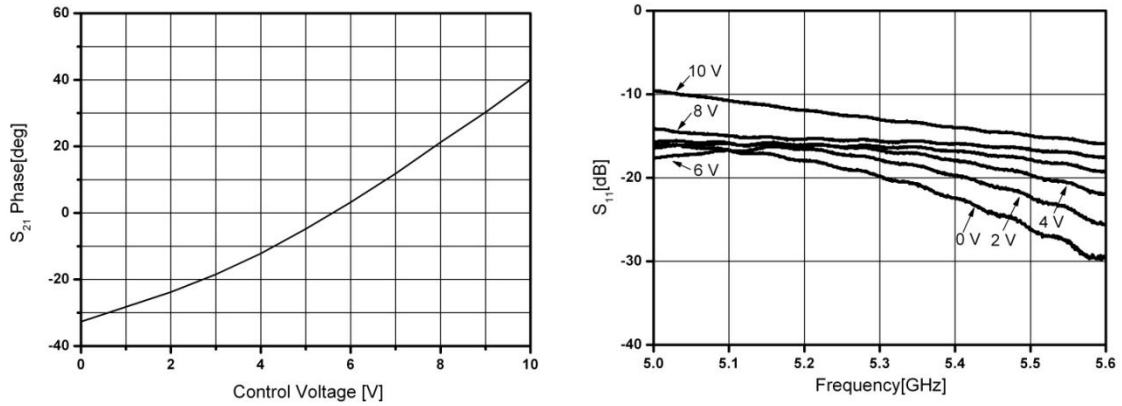
Here, ω_o and Z_o represent the oscillation frequency and 50 ohm, respectively.



(a) (b)

Figure 10.86 (a) Phase shifter circuit: L_1 and L_2 are varactor diodes, resistor R_1=R_2=R_3=1 kohm, capacitor values are C_1=0.3 pF, C_2=0.4 pF, C_{T1}=0.33uF, C_{B1} and C_{B2} are high frequency 100 nF DC block capacitors. (b) Phase shifter layout

The computed values of C_1 and C_2 are approximately 0.3 pF and 1.2 pF and based on these values, the capacitor values can be tuned in ADS simulation to achieve a phase-shift of 70°. The value of C_2 is adjusted to 0.4 pF while the value of C_1 is similar to the computed value 0.3 pF. Figure 10.86(b) shows the layout of the phase shifter circuit. Wafer probe pads were inserted in the phase shifter layout to enable the independent S-parameter measurement of the phase shifter as in the case of the amplifier. The wafer probe pads are shown as ● in Fig. 10.86(b).



(a) (b)

Figure 10.87 (a) The measured phase tune characteristic and (b) return loss with respect to DC tuning voltage

Figure 10.87(a) and (b) show the measured results of the fabricated phase shifter. Figure 10.87(a) shows the amount of phase shift with respect to the varactor diode tuning voltage. The varactor diode tuning voltage was varied between 0 ~ 10 V. As expected, a phase shift of about 72° can be obtained. Figure 10.87(b) shows the measured return loss, dB(S_{11}). The return loss can be seen to vary according to the varactor diode DC tuning voltages. It can be seen that all the return losses are below 10 dB within the oscillation frequency band, which does not cause a serious mismatch in cascade connection to other components.

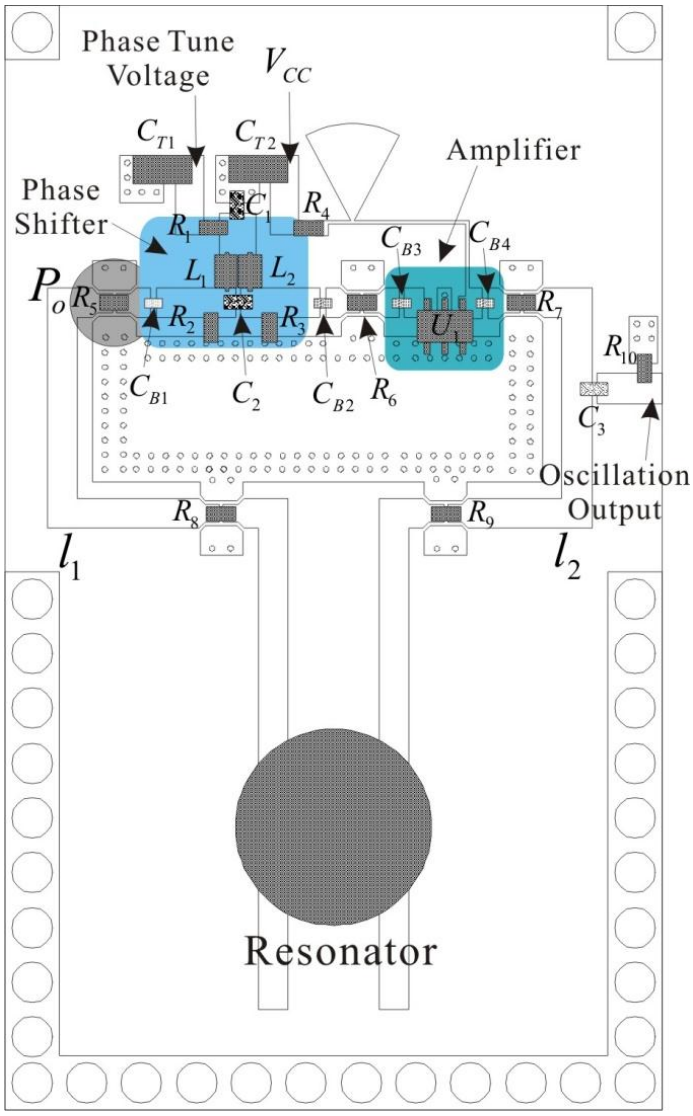


Figure 10.88 The dielectric resonator oscillator layout (44 × 72mm^2)

Figure 10.88 shows the layout of the oscillator which includes each of the separately designed and measured components. It can be seen from Fig. 10.88 that the layout is designed to allow the independent S-parameter measurements of each block such as the resonator, amplifier, and phase shifter using wafer probe. After measurement is carried out for each component, the components are connected in cascade soldering 0 ohm resistors R_5, R_7, R_8 and R_9 in Fig. 10.88 to the wafer probe pads. In this way, a closed-loop oscillator can be formed.

The 50 ohm microstrip lines l_1 and l_2 in Fig. 10.88 are deliberately inserted to make the sum of the phase of the open-loop gain to be an integer multiple of 360° at the oscillation frequency of 5.3 GHz. The oscillation output is obtained through capacitor C_3. Resistor R_{10}, whose value is 50 ohm, is inserted to enable the measurement of the open-loop gain. Rather than the 50 ohm resistor, a 50 ohm coaxial termination can be also used to measure the open loop gain. After disconnecting one of the resistors R_5, R_7, R_8 and R_9 in Fig. 10.88, the open-loop gain can be measured using wafer probes by placing wafer probes on the disconnected wafer probe pads.

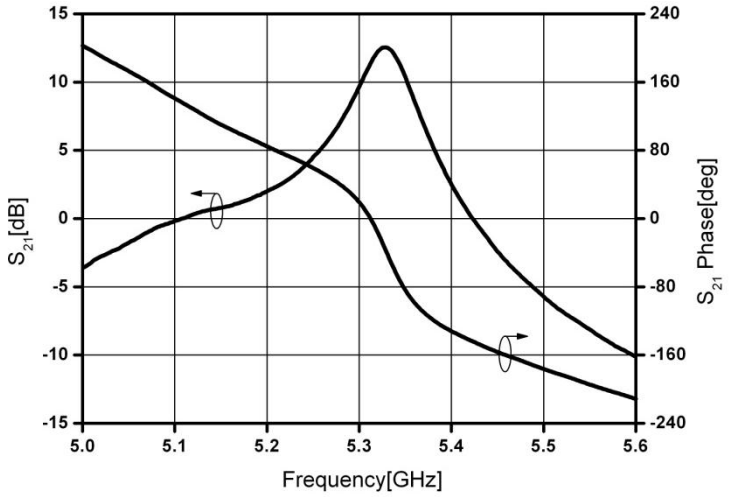


Figure 10.89 The measured loop gain (the DC phase tune voltage of the phase shifter is set to 6 V)

Figure 10.89 shows the measured open-loop gain using Agilent E8358A network analyzer. In Fig.10.85, the phase tune voltage is set to 6V, which corresponds to the center value of DC phase tune voltage. This voltage 6V also corresponds to about the center frequency of the oscillator. At the phase tune voltage of 6V, the magnitude of the open loop gain, S_{21} is greater than 0 dB at the center frequency of 5.3 GHz, and the phase can be seen to be 0° at a frequency of 5.313 GHz. Therefore, the oscillation frequency can be expected to occur at 5.313 GHz, close to 5.3GHz. The group delay can be obtained by calculating the slope at the frequency where the phase is 0°. Thus, the group delay is

$$t_g = \left.\frac{\partial\phi}{\partial\omega}\right|_{\omega=\omega_o} = -\frac{4.106-(-11.298)}{2\pi(5.31-5.318)\times 10^9}\times\frac{\pi}{180} \cong 2.5 \text{ nsec}$$

The DRO is formed by closing the open-loop. Figure 10.90 shows the photo of the fabricated DRO. The photo was taken after removing the metal box enclosure of the dielectric resonator. The DC voltage and phase tune voltage were applied through the coaxial connector, which is to minimize the noise from outside.

The characteristics of the DRO can be measured with a spectrum analyzer, however, for more precise measurements, Agilent E5052A signal source analyzer was used for the measurement. The measured results are shown in Fig. 10.91. Figure 10.91(a) show the oscillation frequency change with respect to the phase tune voltage. The electrical frequency tuning range was measured to be 99 MHz (5.264 ~ 5.363 GHz) at the phase tune voltage change of 0 ~ 10 V. The electrical frequency tuning range expected from the group delay which is obtained from the open-loop gain measurement. From equation (10.62), the electrical frequency tuning range is calculated to be

$$\Delta f = \frac{\theta}{t_g} = \frac{36}{2.5n}\times\frac{1}{180} = 0.08 = 80 \text{ MHz}$$

This shows a difference of 19 MHz, which is due to the approximate computation in the previously group delay. Note that the electrical frequency tuning characteristic appears to be the same as the phase tune characteristic of the phase shifter from equation (10.62). Thus, the closer the phase tune

characteristic of the phase shifter is to a straight line, the more linear the electrical frequency tuning characteristic appears to be. Therefore, in order to have a linear frequency tuning characteristic, a phase shifter with linear phase tune characteristic should be implemented.

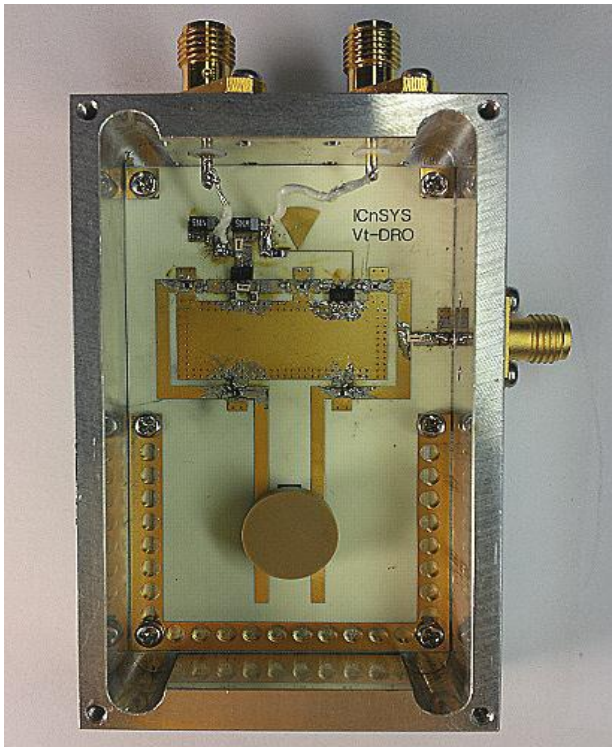


Figure 10.90 Photo of the fabricated dielectric resonator oscillator (44 × 72 × 22mm^3)

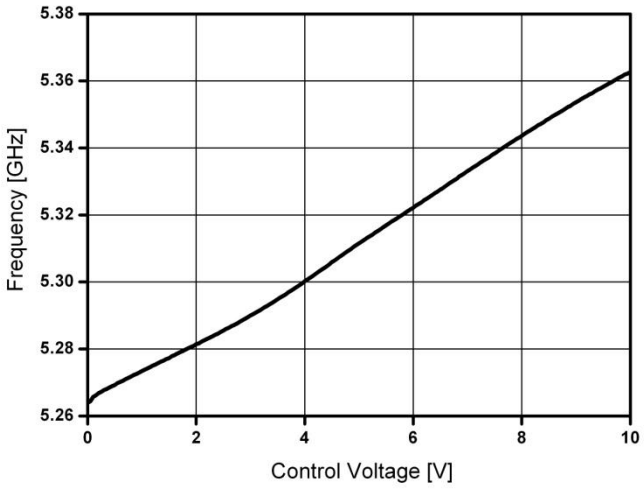
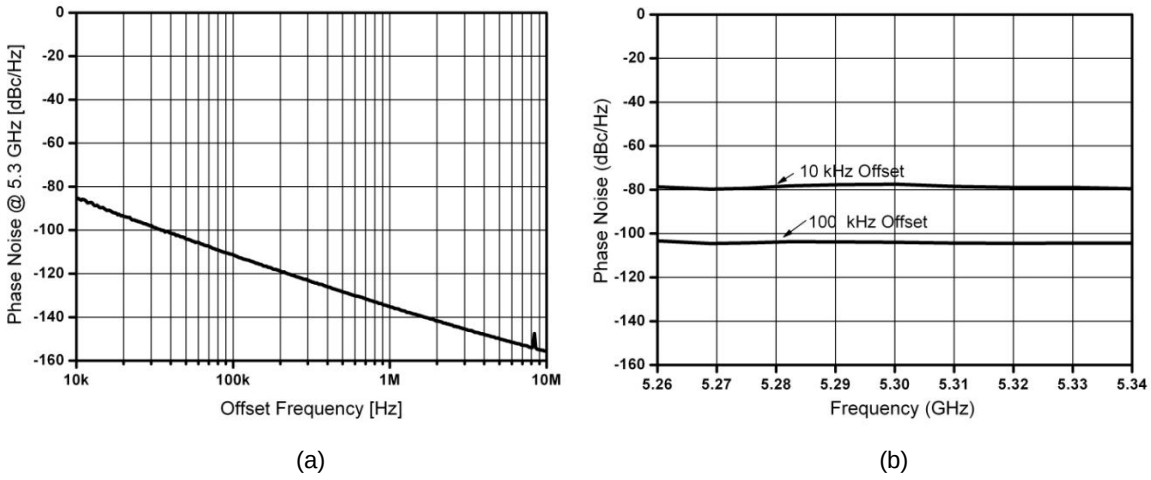


Figure 10.91 Frequency tuning characteristic of the fabricated dielectric resonator oscillator

Figure 10.92 shows the phase noise characteristics. Figure 10.92(a) is the phase-noise characteristics at the center frequency of 5.3 GHz, which appear when the phase tune voltage is about 6V. In Fig. 10.92(a), the phase noise can be seen to be about –111 dBc/Hz at the offset

frequency of 100 kHz. Figure 10.92(b) shows the phase noise when the phase tune voltage was varied with the offset frequency fixed to 100 kHz. From the figure, even though the phase tune voltage is changed, the phase noise can be seen to remain constant. Note that when the phase tune voltage is changed, the phase of the open-loop gain changes; however the group delay does not change because the group delay is chiefly determined by the resonator. As a result, regardless of the change in the phase tune voltage, a constant phase noise is displayed due to an approximately constant group delay. Generally, when the resonant frequency of the resonator is tuned using a frequency tuning device, such as varactor diode, the *Q* of the resonator varies according to the resonant frequency change. Therefore, when the resonant frequency of the resonator is directly tuned using a frequency tuning device, the phase noise varies according to variation in the oscillation frequency. However, when the oscillation frequency is tuned using a phase shifter, the *Q* of the resonator does not change and a constant phase noise is obtained regardless of the tuning of the oscillation frequency.



(a) (b)

Figure 10.92 Frequency tuning characteristics of the fabricated DRO: (a) Phase noise characteristics at oscillation frequency of 5.3 GHz, and (b) phase noise at offset frequency of 10 kHz and 100 kHz when the phase tune voltage was varied

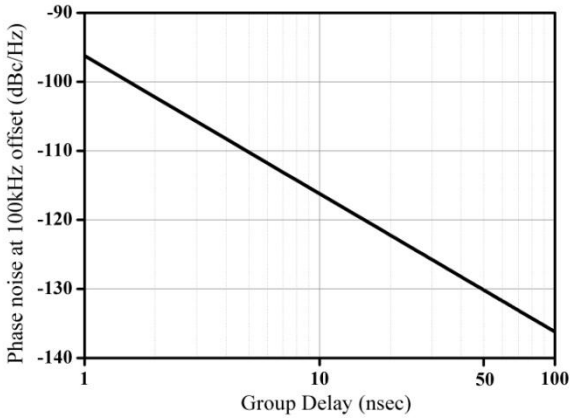


Figure 10.93 Phase noise with respect to group delay at a frequency offset of 100 kHz

There are often many applications that require further improvement in phase noise rather than wide electrical frequency tuning range. From equations (10.63) and (10.64), increasing the group delay of the resonator leads to a narrower electrical frequency tuning range and improved phase noise. The improvement in phase noise can be estimated using equation (10.65) for an increased group delay with the basic configuration of the oscillator unchanged. Figure 10.93 shows the variation of the phase noise with respect to group delay based on equation (10.65). In Fig. 10.93, a resonator with more than 50 nsec group delay (approximately 20 times improvement in group delay of the previous DRO) results in DRO with a phase noise of less than -130 dBc/Hz at 100 kHz offset frequency. Now, we will investigate the design of a resonator with a group delay of more than 50 nsec in order to obtain a phase noise of -130 dBc/Hz and verify the performance of a DRO with the resonator having a group delay of more than 50 nsec.

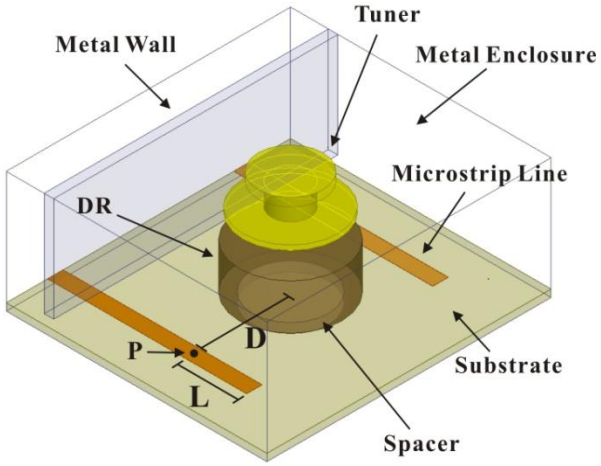


Figure 10.94 Definition of parameters for resonator for improving the group delay

Figure 10.94 shows a resonator configured with dielectric resonator identical to that of Fig. 10.82. The group delay of the resonator mainly changes according to the distance between the microstrip and the center of the resonator (D) and the length extension (L) of the microstrip from the center of the dielectric resonator as shown in Fig. 10.94. The width of the microstrip line can also be a variable for improving the group delay. However, mismatch between the already designed phase shifter and amplifier may be caused by width change which necessitates the width to be fixed to that of 50 ohm impedance as in Fig. 10.82.

Figure 10.95 shows the variation of group delay with respect to D and L defined in Fig. 10.94. The group delay increases with increasing distance D and is lowest near L = 7 mm. Other parameters of interest in the improvement of the group delay are return loss and insertion loss which also depend on D and L. A high insertion loss requires a high gain amplifier since oscillation will not occur without the high gain amplifier even though the group delay is high. Furthermore, when the return loss is small, the open-loop gain cannot simply be expressed as S_{21}due to the mismatch between other components such as phase-shifter and amplifier and the mismatch must be taken into account in the design process, which makes the design difficult.

The results of Fig. 10.95(a) are related to the coupling between the dielectric resonator and the microstrip. It can be found that the group delay increases with increasing distance D. As D increases, the magnetic field from the microstrip becomes weaker and the coupling caused by the magnetic field intensity from the microstrip decreases. Note that the coupling of the microstrip makes the loaded Q, Q_L decrease from Q_u of the dielectric resonator. Thus, Q_L increases as the

coupling becomes smaller, thereby increasing group delay. The group delay variation with respect to *L* can be understood from the current standing wave pattern. Since the end of the microstrip line is open, the current is a maximum at point P when point P is placed away from the microstrip end by 1/4 wavelength (*L* = 7.4 mm). Thus, the coupling by the microstrip magnetic field is maximum and the group delay is minimum at *L* = 7.4 mm. The group delay increases when *L* increases or decreases from the 1/4 wavelength as the current corresponding to the magnetic field at point P decreases when *L* is away from 1/4 wavelength.

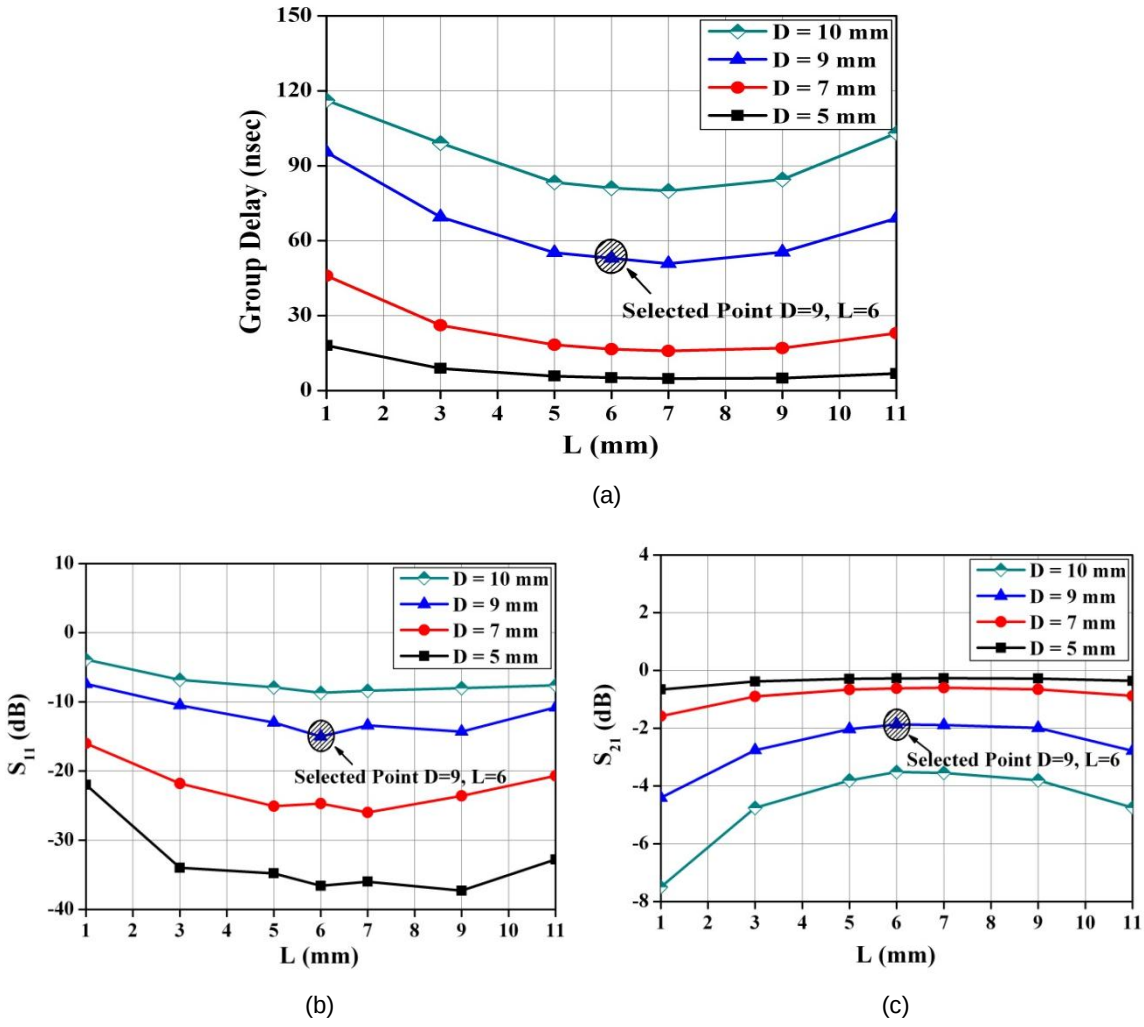


Figure 10.95 Simulation results of resonator part (a) group delay (b) return loss (c) the insertion loss of the delay

Figure 10.95(b) shows the variation of the return loss, which is similar to the variation of the group delay in Fig.10.95(a). A smaller coupling means a smaller power delivered to the dielectric resonator from the power incident at the microstrip. Thus, most of the power is not delivered but rather reflected because the microstrip end is open. This results in higher return loss as the group delay increases. The insertion loss shown in Fig. 10.95(c) can be interpreted similar to the return

loss. Therefore, the increased group delay necessarily accompanies both a larger insertion loss and smaller return loss. When an insertion loss below 3 dB and a return loss greater than 10 dB are allowed for the DRO design, a distance D = 9 mm, and L = 6 mm was found to be appropriate and the resulting group delay was 53 nsec.

The expected phase noise, from the design parameters and using equation (10.65) is –132 dBc/Hz, and the electrical frequency tuning range is calculated to be 5 MHz. Compared to the previous DRO design, the phase noise at an offset frequency of 100kHz is computed to be improved by approximately 26 dB and the frequency tuning range can be seen to have been reduced by about 1/20. Figure 10.96 shows the photograph of the DRO with the newly designed resonator. In this photograph, only the resonator has been changed and the remaining parts are the same as in the previous DRO circuit.

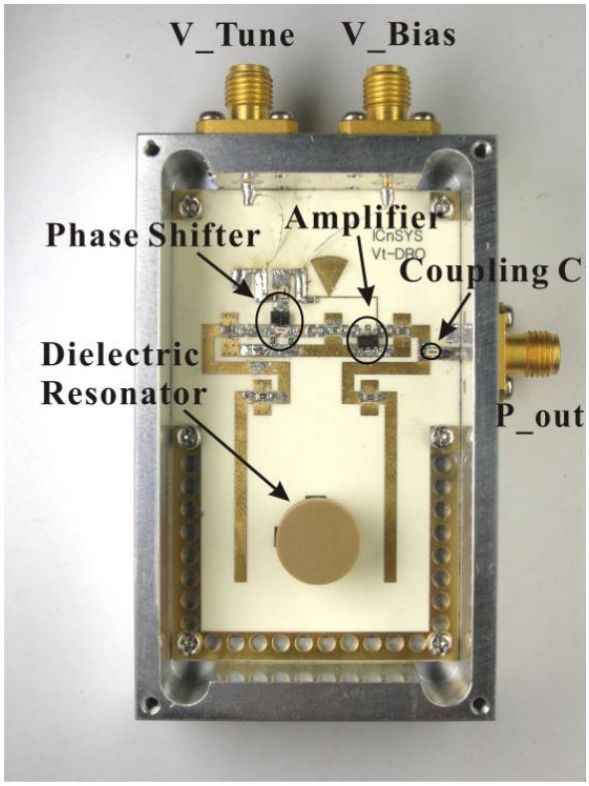


Figure 10.96 Fabricated DRO (44×72 ×22 mm^3) with the improved resonator

Figure 10.97 shows the measured results for the newly designed DRO using signal source analyzer E5052A from Agilent. The measured electrical frequency tuning range is found to be approximately 5 MHz at a phase tune voltage of 0 ~ 10 V. Approximately, 4.5 dBm output power was measured at a phase tune voltage of 6 V. The phase noise against frequency offset is shown in Fig. 10.97(a) and the phase noise at a frequency offset of 100 kHz was measured to be –132.7 dBc/Hz. This result can be seen to be close to the results predicted using the group delay. Figure 10.97(b) shows the variation of the phase noise with respect to oscillation frequency at a constant frequency offset. Although the oscillation frequency changes, it can be seen that the phase noise is flat. The advantage of the loop type DRO where the oscillation frequency is controlled using the phase shifter appears in Fig. 10.97(b); that is, the phase noise at a given constant frequency offset is constant even when the oscillation frequency changes.

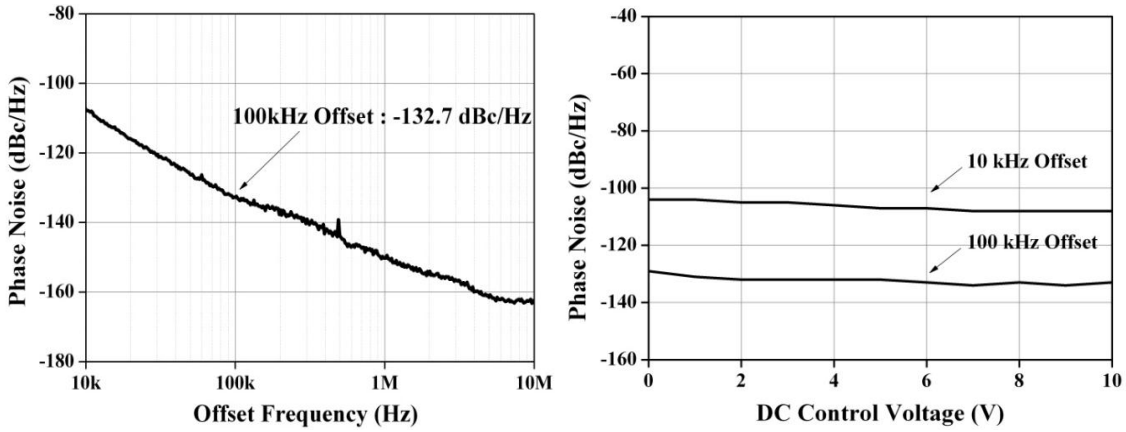


Figure 10.97 Measured results of the fabricated DRO employing the improved resonator; (a) frequency tuning characteristic, (b) phase noise at a phase tuning voltage of 6V, and (c) phase noise with respect to oscillation frequency at a fixed offset frequency

10.6.3.3 Comparison between the two DRO design methods

We have so far looked at two design methods. One is to design a DRO employing a dielectric resonator in the feedback network of the oscillator and the other is the reflection type method (the design method of 10.6.3.2) which replaces the reactance x or y with a dielectric resonator coupled microstrip circuit. There is no superiority between the two configurations in terms of phase noise. From the design point of view, the phase noise of the reflection type may not be systematically improved, and currently does not also provide a systematic way of oscillation frequency tuning. On the other hand, in the case of the feedback type, it is easy to design, and the phase noise and electrical frequency tuning range can be systematically improved.

REFERENCES

[1] M. Randall and T. Hock, "General oscillator characterization using linear open-loop S-Parameters," *IEEE Transactions on Microwave Theory and Tech.*, vol. 49, no. 6, pp. 1094-1100, June 2001.

[2] R. Rhea and B. Clausen, "Recent trends in oscillator design," *Microwave Journal* Jan., 2004.

[3] M. Maeda, K. Kimura, and H. Kodera, "Design and performance of X-band oscillators with GaAs Schottky-gate field effect transistors," *IEEE Trans. on Microwave Theory and Tech.*, vol. 23, August, 1975.

[4] C. Raucher, "Large-signal technique for designing single frequency and voltage controlled GaAs FET oscillators," *IEEE Trans. on Microwave Theory and Tech*., vol. 29 pp. 293-304, April, 1981.

[5] M. Q. Lee, S. J. Yi, S. Nam, Y.K. Kwon, and K. W. Yeom, "High frequency harmonic loaded oscillator with low bias using a nonlinear design approach," *IEEE Trans. on Microwave Theory and Tech*., vol 47, pp. 1670-1679, Sept., 1999.

[6] G. D. Vendelin *et al*., *Microwave Circuit Design using linear and nonlinear techniques*, John Wiley & Sons Inc., 1990.

[7] W. P. Robins, *Phase noise in signal sources*, IEE Press, 1984.

[8] D. B. Lesson, "A simple model of feedback oscillator noise spectrum," *Proc. of the IEEE Lett*., pp. 329-330, Feb., 1966.

[9] R. A. Pucel and J. Curtis, "Near carrier noise in FET oscillators," in *IEEE MTT-S Int. Symp. Dig*., pp. 282-284, 1983.

[10] D. Kajfez and P. Guillon, *Dielectric Resonators*, Dedham: MA, Artech House, 1986.

[11] R. Boneti and A. Atia, "Analysis of Microstrip Circuits Coupled to Dielectric Resonators," *IEEE Trans. Microwave Theory Tech.*, vol. 29, no. 12, pp. 1333-1337, Dec. 1981.

[12] J. Brand and J. Ronnau, "Practical Determination of Dielectric Resonator Coupling Coefficients," *Microwave Journal*, pp. 141-144, Nov. 1986.

[13] P. Champagne, "Better Coupling Model of DR to Microstrip Insures Repeatability," *Microwaves & RF*, pp. 113-118, Sept., 1987.

[14] Jeong Hae-chang, Oh Hyeon-Seok, Yang Seong-Sik, and Yeom Kyung-Whan "Design of dielectric resonator oscillator with extended electrical frequency tuning range based on the open loop method," *J. of KIEES*, vol. 20 no. 6, pp. 570-579, June 2009.

[15] Son Bom-Ik, Lee Seok-Jeong, Yeom Kyung-Whan "Design of a Low Phase Noise Vt-DRO Based on Improvement of Dielectric Resonator Coupling Structure," *Journal of KIEES*, vol. 23, no. 6, pp. 691-699, June, 2012

[16] L. Chen, R. Forse, A. H. Cardona, T. C. Watson, and R. York, "Compact analog phase shifters using thin-film(Ba, Sr) TiO3 varactors," *IEEE MTT-S International Microwave Symp.*, pp. 667-670, June 2007.

PROBLEMS

10.1 Plot the real and imaginary parts of the following load impedance, Z with respect to frequency, and also plot the real and imaginary parts of its admittance Y with respect to frequency.

$$Z = r\left\{1 + jQ\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)\right\}, \qquad Y = \frac{1}{Z}$$

Denoting the impedance of the active part as $Z_A = -R$, and that $R > r$; show that the series oscillation condition is satisfied. On the hand, show that, for such active part and a load, parallel resonance condition is not satisfied.

10.2 Given that the oscillation equilibrium conditions are satisfied at the reference plane A–A', prove that the oscillation equilibrium conditions are satisfied even when the reference plane is changed to B–B'. In other words, the oscillation equilibrium is established everywhere in the circuit regardless of the reference plane.

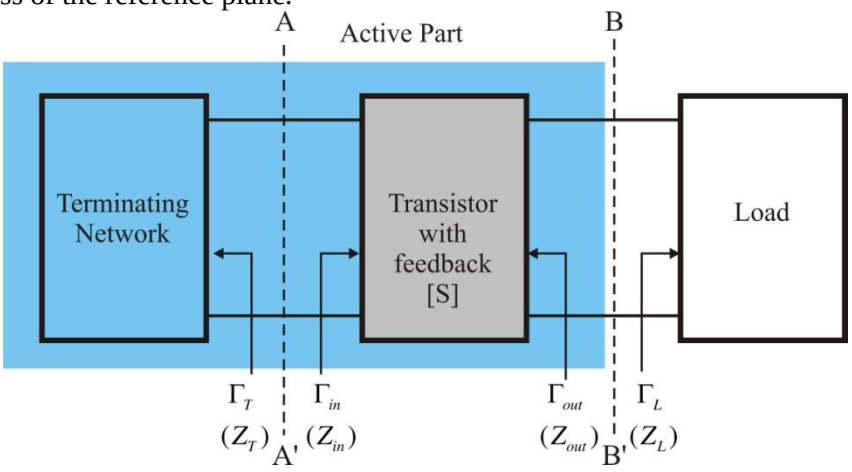


Figure 10P.1 The circuit for Problem 10.2

10.3 Determine S_{11} in polar format for the following circuit at a frequency of 10 GHz.

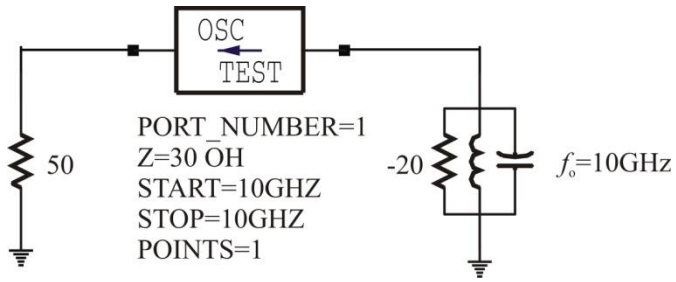


Figure 10P.2 The circuit for Problem 10.3

10.4 Configure the series oscillating circuit of Example 10E.4 in ADS and investigate the effect of the reference impedance on the oscillation condition by varying the reference impedance of **OscTest**.

10.5 In the following measurement, determine the phase noise at a 100 kHz offset from the center frequency and also calculate the maximum phase deviation φ from this offset frequency.

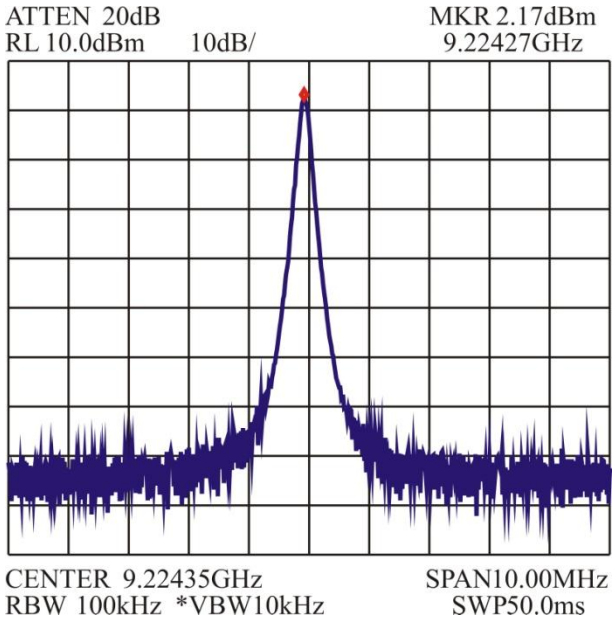


Figure 10P.3 The measured spectrum for Problem 10.5

10.6 Figure 10P.4 is an oscillator circuit operating at 500 MHz~2 GHz. Simplify this circuit to the basic parallel feedback oscillator circuit and calculate the oscillation frequency and the values x, y, Y_L of this parallel feedback oscillator circuit.

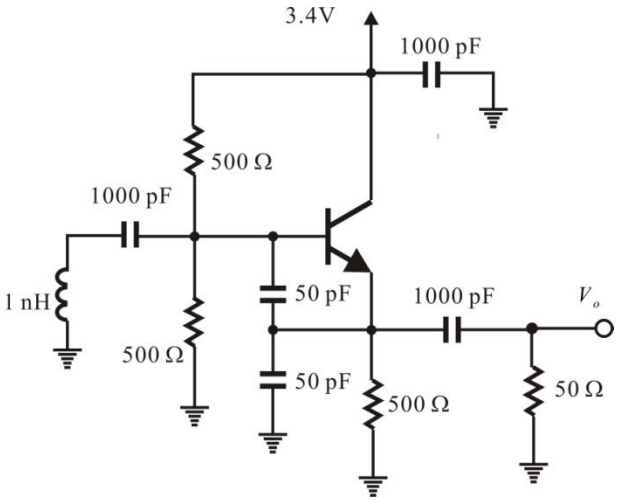


Figure 10P.4 The circuit for Problem 10.6

10.7 Using the large signal model of transistor NE42484, perform the load-pull simulation at 1 GHz and determine the feedback circuit giving optimum power. Furthermore, verify the output power using ADS.

10.8 In the following circuit, assuming that the impedance of the active part changes linearly with the amplitude of RF current,

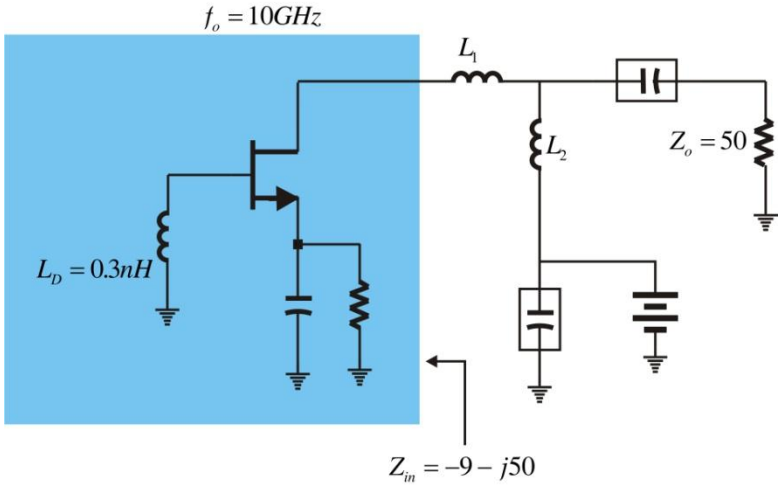


Figure 10P.5 The circuit for problem 10.8

(1) Set the load impedance value to give maximum output power, and calculate the values of L_1 and L_2 to give this value.
(2) Given that the L_D of the active part in the above circuit is to be replaced using a dielectric resonator coupled to a microstrip as shown in the figure below, determine the value of θ. Assume the DR is strongly coupled to the microstrip.

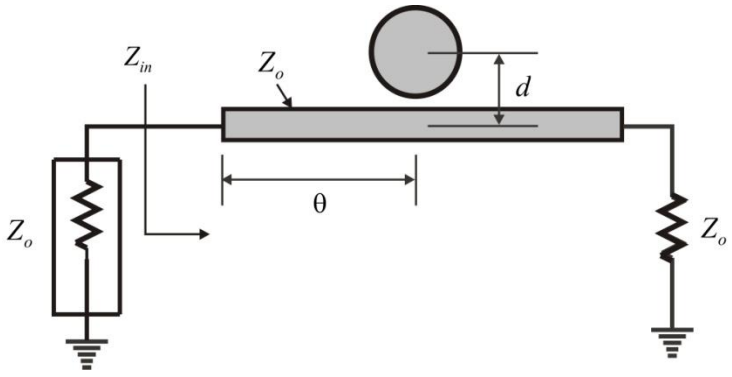


Figure 10P.6 Dielectric resonator coupled microstrip circuit