CHAPTER 5

Introduction to Microwave Active Devices

CHAPTER OUTLINE

5.1 GaAs MESFET
5.2 BJT(Bipolar Junction Transistor)
5.3 DC Bias Circuit
5.4 Small-Signal Equivalent Circuit of FET

INTRODUCTION

Before 1970, most of microwave semiconductor devices were largely diodes and Si BJTs (Bipolar Junction Transistor). Gunn, IMPATT, varactor, PIN, and Schottky diodes were frequently used in microwave applications. When a reverse-biased voltage is applied to a *pn* junction diode, a depletion capacitance appears in the *pn* junction. Since this depletion capacitance varies according to the reverse-biased voltage, varactor diode is a variable capacitor exploiting this property and is often used in adjusting the frequency of oscillators. In addition, a varactor diode can be used to amplify a weak signal as parametric amplifier the operation of which resembles that of a mixer. Such parametric amplifier played an important role as a low noise amplifier in the past because there were no suitable active devices for amplifier application, especially, low-noise amplifiers. Another diode using *pn* junction is PIN diode. By creating an intrinsic-region (I-region) in the *pn* junction, PIN diode can be formed. The resistance of this I-region in PIN diode varies depending on the DC voltage. Based on this property, electronic switches can be implemented in the microwave region. Furthermore, by combining the PIN diodes with the appropriate lengths of transmission lines, it can also be utilized as a digital phase shifter. A PIN diode can also function as an analog type variable attenuator.

Unlike *pn* junction diode, Schottky diode has for a long time been used in detectors and mixers due to its property of rectification. This diode uses majority carrier diffusion and unlike *pn* diode. Consequently, it has no diffusion capacitance, which is associated with minority carriers which provides various benefits when applied in mixers at high frequencies

Gunn diode and IMPATT diode were mostly used as an active component in oscillator and amplifier until the 1970s. In those days, it was difficult to apply transistors at frequencies higher than 4 GHz. The DC characteristics of these diodes show negative resistance when DC bias is set for the optimum operating point. By using this negative resistance, it was much easier to design oscillators. They can also be used as amplifiers. Since the reflection coefficient of devices with negative resistance is greater than 1, these can be configured as reflection amplifiers in combination with a circulator. However, the problem with these diodes is that, they have poor efficiency, and the problem of heat dissipation must always be considered. Therefore, they were used in constructing circuits which use waveguides that easily adapt to thermal design. Such heat problems become important limiting factor in circuit integration. Another disadvantage of these diodes is that, because they cannot be integrated with other devices in a single process, it is intrinsically difficult to build up complex functioning integrated circuits that need other devices.

Major types of transistors are BJT (Bipolar Junction Transistor) and FET (Field Effect Transistor). BJTs use the two carriers, holes and electrons, and a diffusion mechanism in current flow. BJT controls current flow by raising or lowering barrier height formed at junctions. Number of diffusing carriers depends on barrier height which is attained by altering the DC voltage across the junction. On the contrary, FETs use one majority carrier, electron, and a drift mechanism in current flow. FET forms a channel through which electrons can flow. The number of electrons flowing can be controlled by narrowing or widening the thickness of the channel, which is achieved by controlling the gate voltage. FETs are classified according to their channel formation. There are two major types of channel formation; namely, *enhancement type* and *depletion type*. In the enhancement type, no channel is formed but the channel is formed by applying the adequate gate voltage which leads to the accumulation of carriers in the channel. In the depletion type, the channel with carriers is formed in advance and the gate voltage is used to control the thickness of the channel.

Process based on silicon was the only available process technology for fabrication of transistors until the 1970s. Microwave Si BJTs which improved low frequency BJTs in many ways were uniquely used up to the microwave frequencies. Such Si BJT was however not so good for application at frequencies higher than 4 GHz. In the early 1970s, GaAs MESFET (MEtal Semiconductor FET) or simply GaAs FET was developed with the advance of GaAs compound semiconductor process technology. The electron mobility in GaAs is 6 times faster than in Si. With this electron mobility advantage, GaAs FET can show far more excellent performance than Si transistors. When GaAs FETs are fabricated using the technology of the same degree as in Si process, they can shown 6 times improved performances. With the advent of GaAs FET, Gunn diodes, which were popular until that time, became no longer used in amplifiers and oscillators in microwave frequencies of up to Ku-band, and their application is resigned to the millimeter wave frequencies. Then again, a further improvement of the characteristics of GaAs FET led to the emergence of HEMT (High Electron Mobility Transistor) and pHEMT (pseudo-morphic HEMT). It is possible to construct integrated circuit up to a frequency of 200 GHz with these FETs. Thus, Gunn diodes or IMPATT diodes' future use in the millimeter wave remains unclear.

Three-terminal devices such as BJT and GaAs MESFET have several advantages compared to diodes. They provide the flexibility in circuit design which can be applied to many different components such as amplifiers, oscillators, etc. In terms of efficiency, they are superior to the Gunn diodes or such other diodes. They do not require heat dissipation structures if they are not operated at very high power. They can also be used as switches by controlling the gate or base voltage. In addition to these, the characteristic of varactor diode is inherently included in these devices, and they can be integrated in planar circuits as well. They are superior to other active components in

terms of their advantage in integration. The high-frequency characteristics of these three-terminal devices such as BJT and GaAs MESFET have been developed steadily by many researchers and even to date, their performance have been improving every year with the application of new materials or new operating principles.

Therefore, in this chapter we will briefly investigate the behavior and characteristics of these transistors used in microwave applications. Among diodes, we would also look at the varactor diode in oscillator design. The operating principles and performance of Schottky diodes will also be discussed in the mixer design in Chapter 12.

5.1 GaAs MESFET

5.1.1 Operation and Equivalent Circuit

A top planar view of a GaAs FET whose gate length is 0.3 μm and gate width, 250 μm is shown in Fig. 5.1. The cross-section at A-A' of Fig. 5.1 is also shown in Fig. 5.2. In the GaAs FET shown in Fig. 5.2, electron-rich *n*-type epitaxial layer (epi-layer) is grown on the semi-insulating GaAs substrate, on which drain and source terminals are formed as ohmic contacts while the gate terminals are formed as Schottky contact. Thus, when a negative voltage is applied to the gate, the diode between the gate and the epitaxial layer is reverse-biased and no gate current flows. Due to this reverse voltage, a depletion region with no carriers occurs in the epitaxial layer. When the negative voltage applied to the gate is further increased, the depletion region will be widened, which results in narrowing of the channel where electrons can flow. This causes the drain-source current to be further reduced. Therefore the current flowing in the drain-source in this device is controlled through the gate voltage.

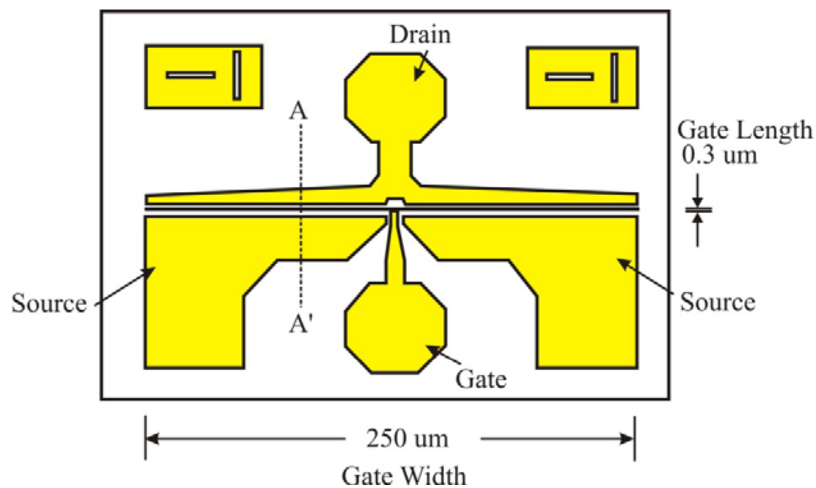


Figure 5.1 A top planar view of GaAs FET

The equivalent circuit of GaAs FET is shown in Fig. 5.2. Resistors R_s and R_d represent the ohmic resistance that occurs from the source and drain ohmic contacts. Resistor R_g represents the gate metallization resistance deposited to form the Schottky junction. The dependence of the drain

current on the gate voltage can be represented by the trans-conductance g_m, and that of the drain current on v_{DS} is represented by the resistance R_{ds}. In contrast with the above R_g, R_s, and R_d, g_m and R_{ds} are non-linear components and they represent the FET's DC characteristics. Resistor R_i is called channel resistance and represents the resistance which occurs in the channel. The depletion region which occurs in the gate region is not directly connected to the source terminal but is connected to the source through a channel region. R_i represents the resistance of such a channel to the source resistance. Capacitors C_{gs} and C_{gd} represent the capacitances caused by the depletion region between the gate and source, and between the gate and drain terminals. The DC bias dependence of these capacitors shows characteristics similar to that of a depletion capacitance. On the other hand, C_{ds} represents the capacitance occurring between the terminals of the source-drain. This capacitance occurs both in the channel and air regions. This also shows nonlinear characteristics, and the characteristic is different from that of the depletion capacitance.

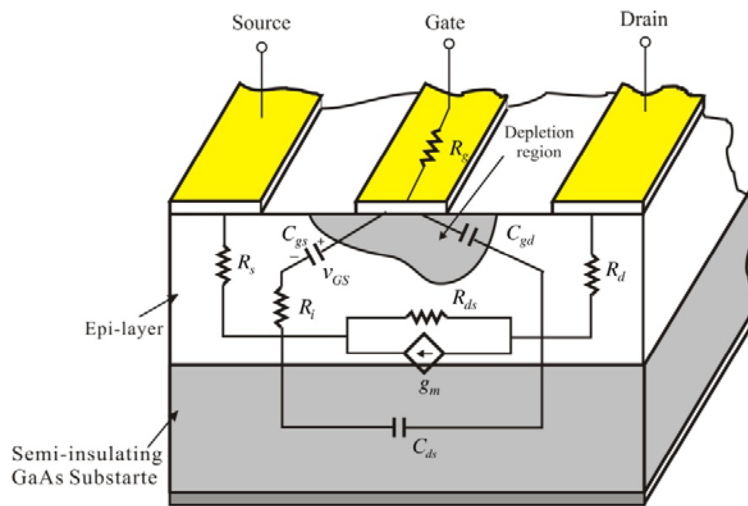


Figure 5.2 Cross-section of GaAs FET and its equivalent circuit

The equivalent circuit in Fig. 5.2 is re-drawn in Fig. 5.3. The trans-conductance is expressed as $y_m = g_m e^{j\omega\tau}$ because the drain current flows with a time delay of τ compared to the gate-source control voltage.

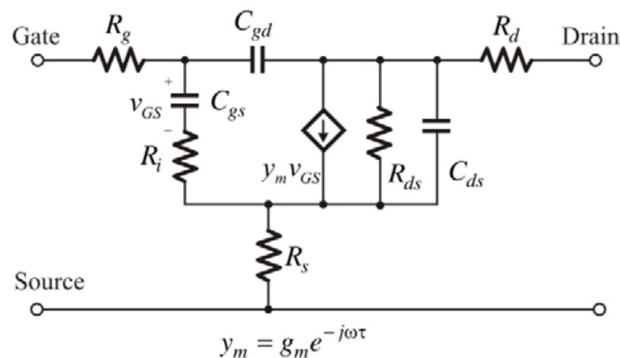


Figure 5.3 GaAs MESFET equivalent circuit

5.1.2 Large-Signal Equivalent Circuit

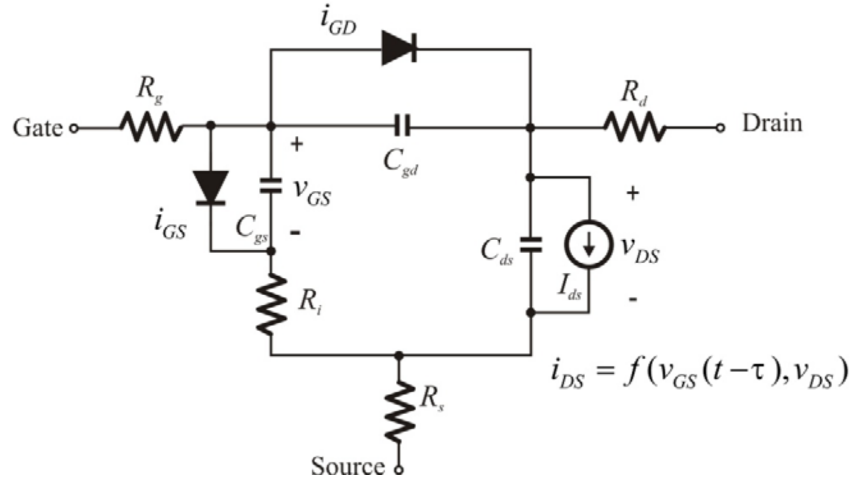


Figure 5.4 Large-signal equivalent circuit

Figure 5.4 shows a large-signal equivalent circuit of GaAs FET. Since the physical origin of R_g, R_s and R_d is itself linear, these circuit elements can be treated as linear devices. The physical operations of the gate-source and the gate-drain junctions can be thought of in terms of Schottky diodes, and i_{GD} and i_{GS} can be described by the following Schottky diode characteristics shown in equations (5.1) and (5.2). By measuring the forward DC current characteristics of the diode, the parameters, such as ideality factor η and saturation current I_s, can be determined.

$$i_{GS} = I_{s1}\left(e^{\frac{v_{GS}}{\eta V_T}} - 1\right) \tag{5.1}$$

$$i_{GD} = I_{s2}\left(e^{\frac{v_{GD}}{\eta V_T}} - 1\right) \tag{5.2}$$

Also, since C_{gs} and C_{gd} are the capacitance of the depletion region, they can be determined by measuring the C–V characteristics given by (5.3) and (5.4) below:

$$C_{gs} = \frac{C_{gs0}}{\left(1 - \frac{v_{GS}}{\phi_{GS}}\right)^{m_S}} \tag{5.3}$$

$$C_{gd} = \frac{C_{gd0}}{\left(1 - \frac{v_{GD}}{\phi_{GD}}\right)^{m_D}} \tag{5.4}$$

On the contrary, the non-linear characteristics of C_{ds} and R_i are not so significant, and the small-signal values of C_{ds} and R_i can be used in the large signal model. The DC characteristics of the drain current which depends on voltage between the gate-source and drain-source are as shown in Fig. 5.5 below. However, the nonlinear characteristics of this device is different from that of the low frequency FET devices, therefore a new mathematical model is required to represent its characteristics.

Mathematically, there are various ways of presenting this result, but of these, there are three well-known mathematical models.

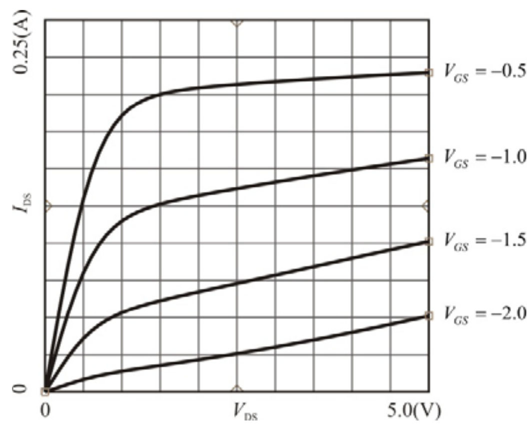


Figure 5.5 I_{DS}-V_{DS} characteristics

The Curtice model describes the characteristics shown in Fig. 5.5 by the equation $(1+\lambda V_{DS})\tanh(\alpha V_{DS})$. The function $\tanh(x)$ approaches 1 as $x\to\pm\infty$, and it can be approximated by x when x is small. Thus, for small V_{DS}, the equation behaves as a straight line for V_{DS} because $(1+\lambda V_{DS})\tanh(\alpha V_{DS}) \cong \alpha V_{DS}$, which steeply increases for V_{DS}. On the contrary, for sufficiently large V_{DS}, the equation can be approximated as $(1+\lambda V_{DS})$, which is approximately constant and increase slightly for V_{DS}. Thus, the I_{DS}–V_{DS} curves can be represented by this equation through fitting of constants α and λ for V_{DS}.

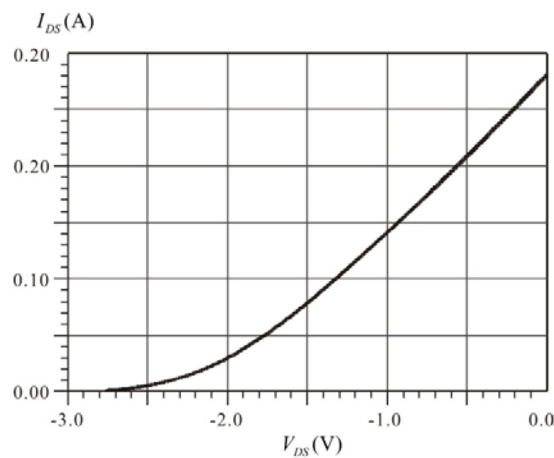


Figure 5.6 I_{DS}-V_{GS} characteristics

On the other hand, since the dependence of the drain current on V_{GS} is close to a parabola shown in Fig. 5.6, this can be modeled using a quadratic equation. However, in reality, the use of quadratic equation does not closely approximate the measured results. The cubic equation given in (5.5) may be better to describe the characteristics in Fig. 5.6 because in it has three degrees of freedom. In addition, the I_{DS}–V_{GS} characteristics depend slightly on V_{DS}. In order to describe this, V_1 instead of V_{GS} which depends linearly on V_{DS} as in equation (5.5b) is used. Thus, the I_{DS}–V_{GS} characteristics are expressed mathematically as follows:

$$I_{DS} = \left(A_0 + A_1 V_1 + A_2 V_2^2 + A_3 V_3^3\right)\left(1 + \lambda V_{DS}\right)\tanh\left(\alpha V_{DS}\right) \tag{5.5a}$$

$$V_1 = V_{GS}\left[1 + \beta\left(V_{DS} - V_{to}\right)\right] \tag{5.5b}$$

For the Materka model, the relationship between drain current and V_{GS} is described in a well-known parabolic relationship, and the slope for V_{DS} is expressed by modifying tanh$x$ in the I_{DS}–V_{DS} characteristics as

$$I_{DS} = I_{dss}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tanh\left(\frac{\alpha V_{DS}}{V_{GS} - V_p}\right) \tag{5.6a}$$

$$V_p = V_{po} + \gamma V_{DS} \tag{5.6b}$$

Note that the pinch-off voltage V_p also depends linearly on V_{DS}.

Raytheon model is a mathematical model developed by Raytheon Corporation and is expressed as follows:

$$I_{DS} = \frac{\beta\left(V_{GS} - V_{to}\right)^2}{1 + \Theta\left(V_{GS} - V_{to}\right)}\left(1 + \lambda V_{DS}\right)\left[1 - \left(1 - \alpha\frac{V_{DS}}{3}\right)^3\right] \tag{5.7}$$

In addition, there are various mathematical models and it is difficult to distinguish them in terms of their pros and cons; but in all, they describe the DC drain current dependences on V_{GS} and V_{DS}. All of them can be used in performing large signal simulation. In addition, it is worth noting that the above equation represents a mathematical relationship for DC characteristics. Since there is time delay of τ in the RF drain current dependence on V_{GS}, large signal microwave operation can be modeled by replacing the above equation with equation (5.8) shown below

$$I_D = f\left(v_{GS}\left(t - \tau\right), v_{DS}\right) \tag{5.8}$$

This can be used as a mathematical model for microwave operation.

5.1.3 Simplified Equivalent Circuit and S-parameters

The equivalent circuit of Fig. 5.3 explains closely the device's physical origin, but it is rather complicated. Resistors R_g, R_s, and R_d are the resistances occurring due to the contacts, and the values of the elements are generally small. Also, they are not an intrinsic part of the FET, and so they are called extrinsic elements. Thus their values are usually approximated to zero, and the resulting approximate simplified small-signal equivalent circuit is shown in Fig. 5.7. This simplified equivalent circuit is used to explain qualitatively and in some cases quantitatively the measured S-parameters of FET and most of the frequency dependence behavior of FET can be explained through the simplified equivalent circuit.

Further approximation for more simplification is possible because the depletion region capacitance C_{gd} is generally small compared to C_{gs}. Sometimes it is also assumed to be 0. Thus, the FET's input and output are isolated; such an approximation is called unilateral approximation.

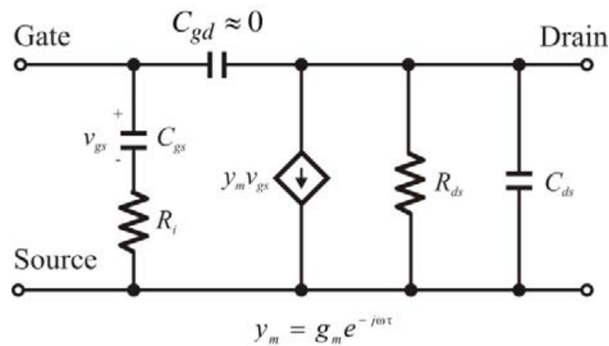


Figure 5.7 A simplified equivalent circuit of FET

Figure 5.8 shows the measured S-parameters of a typical chip state GaAs FET. After GaAs FET chip was assembled by wire-bonding on the carrier shown in Fig. 5.9(b) and (c), the carrier assembly is mounted on a jig as shown in Fig. 5.9(a). In Fig. 5.9(b), the reference planes are shown, and thus the measured S-parameters generally include the inductance of bonding wires.

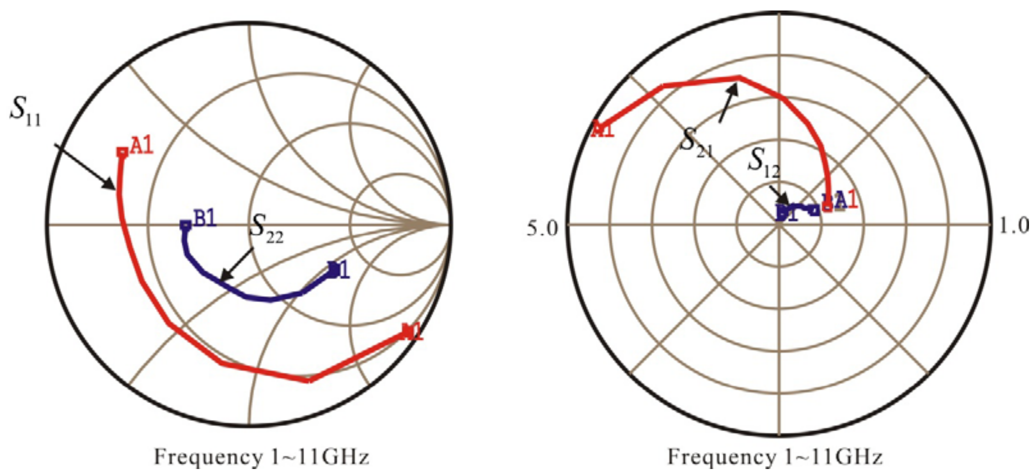
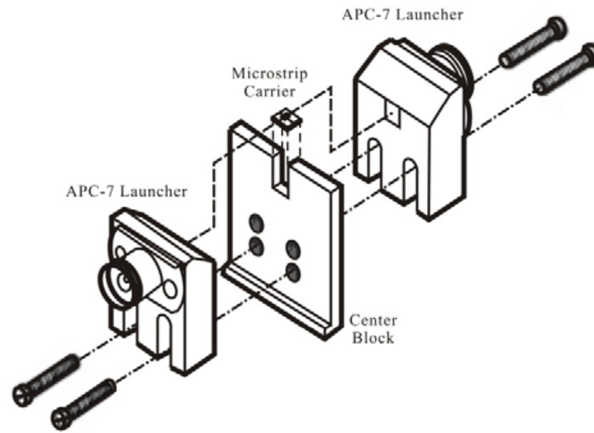
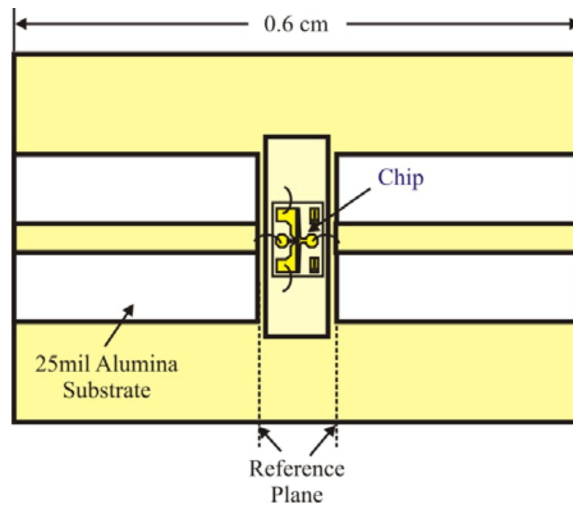


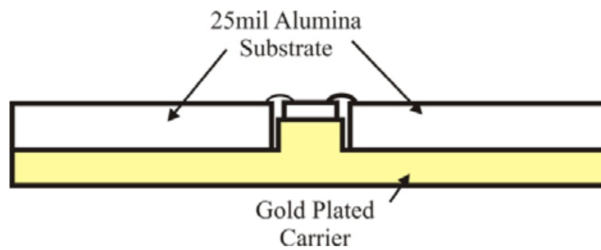
Figure 5.8 Measured GaAs FET S-parameters



(a)



(b)



(c)

Figure 5.9 Illustration of assembly for S-parameter measurement of GaAs FET: (a) Assembly of the test jig, (b) top view of the microstrip carrier, and (c) cross-sectional view of the microstrip carrier[1]

[1] Avantek, High-Frequency Transistor Primer, April, 1968

In Fig. 5.8, S_{11} and S_{22} are related to input and output impedances. Thus, they are generally plotted on the Smith chart as shown. On the contrary, S_{12}, $S_{21}$are the transfer functions and so are plotted on the polar chart showing their magnitude and phase. In Fig. 5.8, the radius is set to 5.0 and the radial division scale is set to 1.0 for S_{21}. On the other hand, as S_{12} is small, the radius is set to 1.0, and the scale is set to 0.2. The frequency response of the S-parameters can be explained using the simplified equivalent circuit shown in Fig. 5.7.

In the unilaterally approximated simplified equivalent circuit, if the input impedance of the FET includes the bonding wire, then we have a series *R-L-C* circuit. Thus the locus of S_{11} lies in a constant resistance circle as frequency increases. At low frequency, the circuit behaves like a capacitive circuit. On the other hand, as the frequency increases, the inductance of the bonding wire becomes dominant, and so the circuit behaves as an inductive circuit. From this, the resistance at resonance corresponds to the channel resistance R_i in the simplified equivalent circuit, but if the ignored contact resistance were to be considered, this will be approximately close to the value R_i+R_g+R_s. In addition, applying the method explained in Chapter 2, the bonding wire inductance and capacitance can be obtained by calculating the *L* and *C* values at resonance. The resulting capacitance and inductance corresponds approximately to C_{gs} and bonding wire inductance.

In the case of S_{22}, the drain-source approximately consists of R_{ds} and C_{ds} in parallel. Therefore, as the frequency approaches 0, the impedance approaches R_{ds}. As the frequency increases, S_{22} moves along a constant conductance circle and the trajectory appears in the capacitive region due to the capacitor C_{ds}. As frequency further increases, S_{22} is observed to move away from the constant conductance circle and to follow approximately a constant resistance circle similar to S_{11} due to the effects of bonding wire inductor and C_{gd}.

In the case of S_{21}, at an extremely low frequency, S_{21} can be computed as

$$S_{21} = -2g_m Z_o = 2g_m Z_o \angle 180° \quad (5.9)$$

Using this, the approximate value of g_m can be found from the low frequency measurement data. As the frequency increase, the voltage across C_{gs} decreases. As a result, $|S_{21}|$ is reduced which corresponds to the voltage across the termination Z_o. In addition, the influence of C_{ds} further reduces $|S_{21}|$. The phase of S_{21} increases in a clockwise direction due to these capacitors.

In the case of S_{12}, when the frequency is extremely low, we can see that S_{12} approximately becomes

$$S_{12} = 2j\omega C_{gd} Z_o = 2\omega C_{gd} Z_o \angle 90° \quad (5.10)$$

From the above equation, it can be found that $|S_{12}|$ increases as the frequency increases. Similar to the phase of S_{21}, the phase of S_{12} can also be seen to increase in a clockwise direction as frequency increases.

5.1.4 Package

When a chip type active device is employed in a circuit, the circuit can be constructed without further performance degradation of the active device. However, active devices can easily be damaged by external environmental factors. Particularly, assembly of chips to PCB is bothersome and inconvenient because PCB mainly uses soldering in the assembly of components. Therefore for convenience of handling, chips are sometimes packaged, and used in packaged form albeit with

some degree of performance degradation. Assembly using a packaged chip can be carried out by soldering and does not require assemblies such as wire bonding and attachment of dies. Also, packaged chip provides the advantage of good protection against the external environment.

Figure 5.10 shows a GaAs FET chip assembled using commercial ceramic package. Figure 5.10(a) shows the top view with the lid removed and (b) shows the back view of the ceramic package. It is generally common to use the source as the ground terminal. To minimize the inductance arising from the assembly of the source terminal, the source terminal is frequently wire-bonded in two places as shown in Fig. 5.10(a). The inductance arising from the assembly of the source terminal, however small, causes feedback from output to input and the possibility of causing oscillation or device instability is high. Thus, to minimize the inductance, the package terminals where the source is connected are usually made wider compared to the other terminals. The chip is mounted directly on the lead terminal, and the source terminals are twice wire-bonded in two places. The heat is thus dissipated through these lead terminals and it is worth noting that such heat dissipation may not be sufficient in some cases.

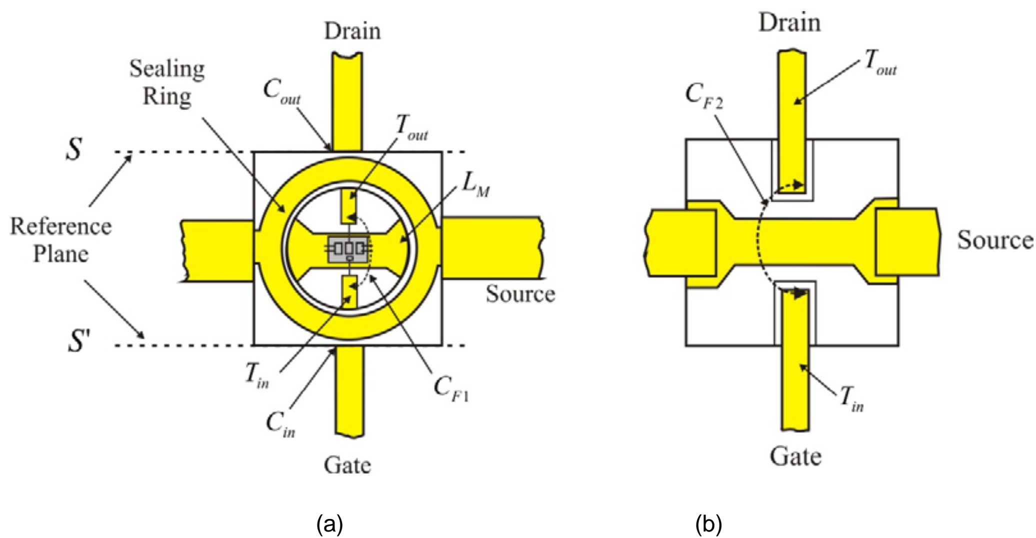


Figure 5.10 GaAs FET package assembly: (a) top view and (b) bottom view

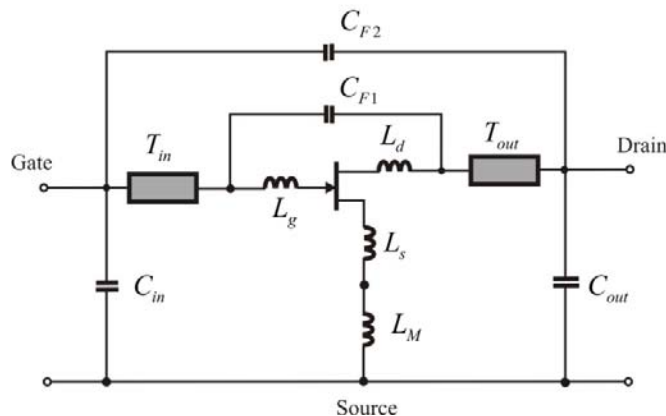


Figure 5.11 Equivalent circuit of the packaged device

The plane S and S' shown Fig. 5.10(a) becomes the reference plane of the S-parameter measurement and the measured S-parameters are generally provided with these reference planes. Thus, many parasitic elements can be formed in the packaged device compared to the chip. This is shown in Fig. 5.11. The bonding wire inductances L_g, L_s, and L_d occur as a consequence of wire bonding. In addition, since lines with a finite length are inserted in the package, these accordingly appear as transmission lines or inductance. The transmission lines T_{in}, T_{out}, and inductor L_M in Fig. 5.11 represent such transmission lines and inductance. Furthermore various parasitic capacitances occur. The capacitance C_{in} and C_{out} occur due to the discontinuity of the transmission lines. The capacitance C_{F1} and C_{F2} represent feedback capacitances occurring due to the coupling between the lines in the package and due to the upper line and the back line respectively.

Such packaging parasitic circuit elements prevent the accurate determination of the values of the active device equivalent circuit. Thus, it is common to obtain firstly the equivalent circuit of the chip and then the equivalent circuit of the package itself. These are combined to obtain the overall equivalent circuit.

5.1.5 GaAs pHEMT

The electron mobility of FET in channel is closely related to the high-frequency performance. The previously explained GaAs FET shows more improved high-frequency performance than Si because the electron mobility in GaAs is about 6 times larger than Si. However, such electron mobility is generally degraded by the impurity doping which is done to generate electrons. The impurity atoms after generation of electrons take on + polarity while electrons take on – polarity. The moving electrons are thus attracted and scattered by the fixed impurity atoms having + polarity. As a result, the electron mobility is significantly degraded by these *impurity scattering*. Such degradation of electron mobility can be avoided employing the complex epitaxial layer structure instead of single epitaxial layer. Figure 5.12 shows the complex epitaxial layer structure to improve the electron mobility.

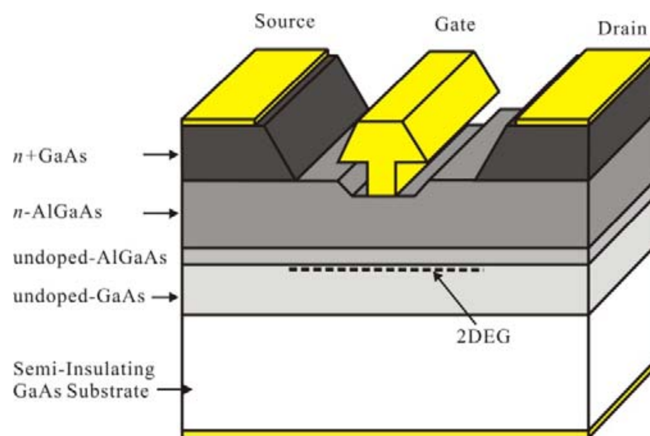


Figure 5.12 Cross-sectional structure of GaAs HEMT

In Fig. 5.12, the electrons are generated in the *n*-type AlGaAs layer, where impurity atoms are richly doped. The hetero-junction is formed between the undoped AlGaAs and the undoped GaAs. As a result, an *electron-well* is due to the hetero-junction. The generated electrons in the *n*-type

AlGaAs layer are then easily trapped and gathered in this electron well formed near undoped GaAs layer. Since the thickness of the electron well is very thin, the trapped electrons in the electron well can be considered as a sheet of electron gas. So it is called as 2DEG (2-Dimensional Electron Gas). In addition, note that the undoped GaAs layer is almost intrinsic because there were no impurity atoms. Thus, the electrons can move according to the applied electric field without the influence of the impurity atoms. This leads to an electron velocity much faster than in GaAs FET. Therefore, the high-frequency performance can be improved compared with conventional GaAs FET because the electrons move much faster in the undoped channel. For such reason, the device is called HEMT (High Electron Mobility Transistor)

In the fabrication of these devices, the lattice constants of the AlGaAs and GaAs differ significantly and so it is difficult to grow a stable AlGaAs layer on the GaAs. The problem is solved using the recently developed *pseudo-morphic* technology. Inserting extremely thin undoped InGaAs layer between undoped GaAs and undoped AlGaAs layers, the stable AlGaAs layer can be grown, which has made it possible to manufacture such high-performance devices. Since the pseudo-morphic technology is employed to fabricate the device, the device is often called pHEMT.

5.2 BIPOLAR JUNCTION TRANSISTOR (BJT)

5.2.1 Operation of Si BJT

The structure of BJT is shown in Fig. 5.13. Figure 5.13(a) shows the top view and (b) shows the cross-sectional view through the line S-S'. As shown in the figure, firstly an *n*-type epitaxial layer is grown on the *n*+ substrate. On the *n*-type epitaxial layer, the base region is formed by locally doping a *p*-type material. The emitter area is then formed by locally doping a n^+-type material on the base region. Through this procedure, an *npn* BJT can be formed.

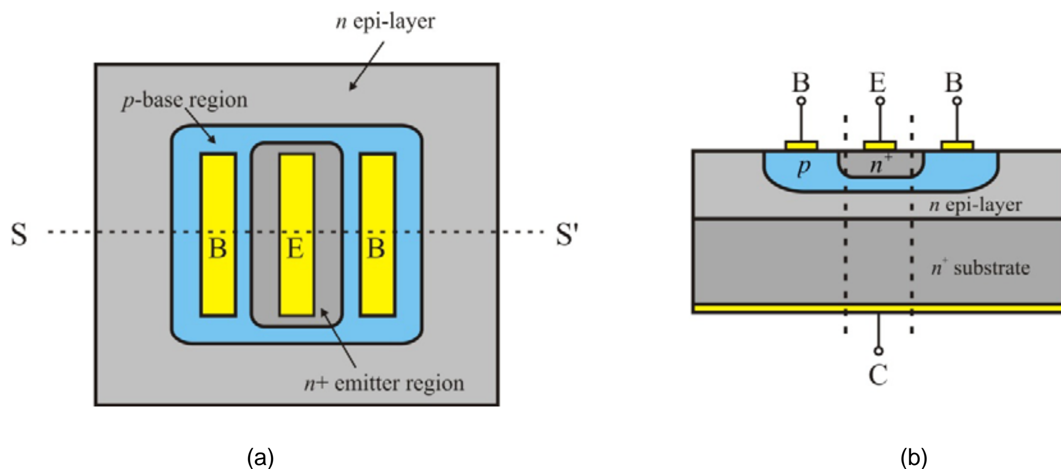


Figure 5.13 Structure of BJT: (a) Top view and (b) cross-section through line S-S'

The principles of operation of *npn* transistor is usually explained using the dotted line area in Fig. 5.13(b). This is shown in Fig. 5.14. Two *pn* junctions appear in the transistor and these two *pn*

junction diodes are connected to back-to-back. The BJT can operate various modes, such as active, cutoff, inverse, and saturation modes. In the active mode, the base-emitter (BE) junction is forward-biased while the collector-base (CB) junction is reverse-biased. In this way, the barrier height of the BE junction is lowered while the CB junction barrier height is raised. Due to the lowered BE junction barrier height, the majority carriers, electrons in the emitter region can diffuse into the base region while the holes in the base region diffuse into the emitter region. On the other hand, because the CB junction is reverse-biased, the diffusion between the collector and base do not appear due to the increased barrier height. Normally, the emitter region is more heavily doped than the base region. Thus, more electrons will diffuse from the emitter to the base than holes from the base to the emitter. Consequently, the current contribution from the diffusion of holes can be neglected.

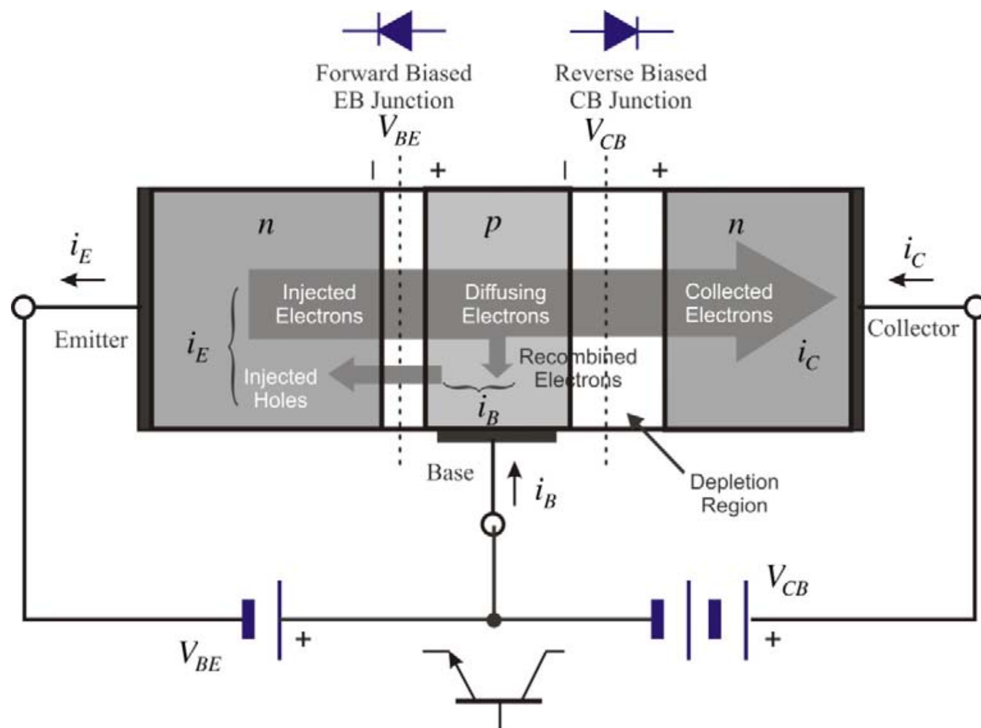


Figure 5.14 Description of the operation principle of *npn* transistor

Small number of the diffused electrons from the emitter recombines and thereby disappears in the base region while most of the electrons reach and are collected in the collector region. Thus the collector current i_C is almost equal to the emitter current i_E. Note that the emitter current i_E depends on the BE junction barrier height, which in turn is controlled by a small voltage applied to the BE junction, V_{BE}. Therefore, the large emitter current flow of BJT can be controlled by a small voltage V_{BE}, thereby acting as amplifier. Thus, the BE junction voltage plays a similar role of the gate-voltage in FET.

However, the structure of the BJT shown in Fig. 5.13(b) needs some improvements in structure to be used for a high frequency application. Basically, high frequency performance is strongly related to the base width. The electrons injected from the emitter should transit the base region to reach the collector. The transit time is related to the base width. Thus, the base width should be as narrow as possible. Secondly a base spreading resistance occurs due to the distance between the true

base region and the actual base terminals (shown in Fig. 5.13(b)). As a result, the gain at high frequencies is reduced. The base spreading resistance can be reduced by increasing the base region doping. However, the significantly increased doping of the base region increases the number of holes and consequently holes diffusing from the base to the emitter increases. As a result, the base current increases, which is not useful. As a way of reducing the base spreading resistance, the base and emitter is implemented using the inter-digital structure shown in Fig. 5.15. When the finger width and spacing of the inter-digital structure are made narrow, the base-spreading resistance can be significantly reduced due to a short length between the true base region and the base terminal.

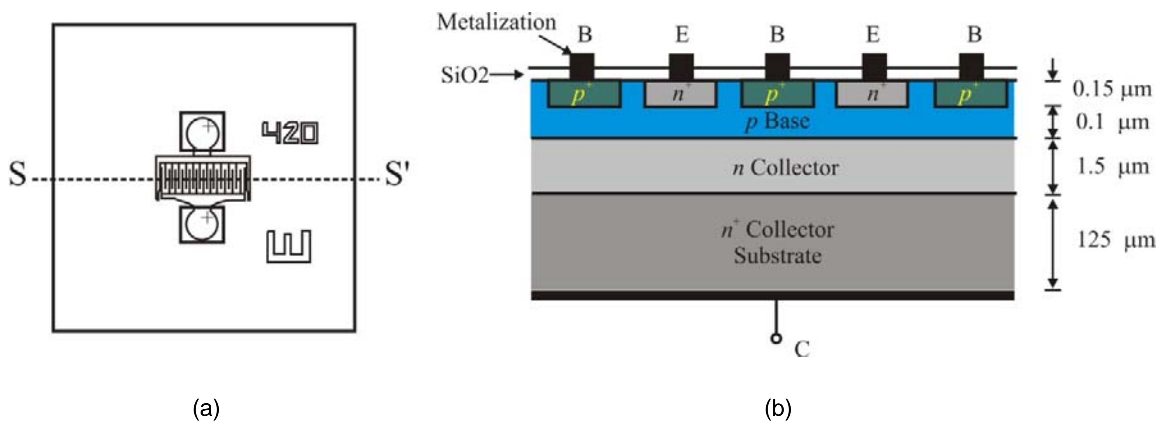


Figure 5.15 High-frequency BJT's (a) top view and (b) cross-sectional views

In addition, because the electrons should pass through the *n*-type epitaxial layer in order to reach the collector terminal, the epitaxial layer is fabricated sufficiently thin to make the electrons arrive at the collector terminal much faster. Such a BJT structure is shown in Fig. 5.15 and the cross-sectional structure along S-S' is shown in Fig 5.15(b). As shown in the figure, the base thickness is typically the order of 0.1 μm, and the *n*-type collector thickness is typically order of 1.5 μm, which is extremely thin. The base and emitter spacing is found to be about 1 μm to reduce the base-spreading resistance.

5.2.2 Large-Signal Model of BJT

Large-signal model of BJT can be illustrated as shown in Fig. 5.16. From Fig. 5.14, since the BE and BC junctions can be represented by diodes, these are represented as diodes I_{BR} and I_{BF} in Fig. 5.16. The subscript B means the base, and F and R stands for forward and reverse. In addition, the space charge region diode is known to occur in the *pn* junction when junction current are in small level. Thus, these space charge region diodes appear in the BE and BC junctions and these diodes are connected in parallel. They are represented by diodes I_{LE} and I_{LC} of Fig. 5.16. It is worth noting that the collector current is not generated due to the space charge region diode currents, and the currents due to these diodes can be treated as leakage currents, which is why the subscript *L* is added. Therefore, the base current can be expressed in terms of the collector saturation current I_s as follows:

$$I_B = \frac{I_S}{\beta_F}\left(e^{\frac{qV_{BE}}{n_F kT}} - 1\right) + \frac{I_S}{\beta_R}\left(e^{\frac{qV_{BC}}{n_R kT}} - 1\right) + C_2 I_S\left(e^{\frac{qV_{BE}}{n_{EL} kT}} - 1\right) + C_4 I_S\left(e^{\frac{qV_{BC}}{n_{CL} kT}} - 1\right) \quad (5.11)$$

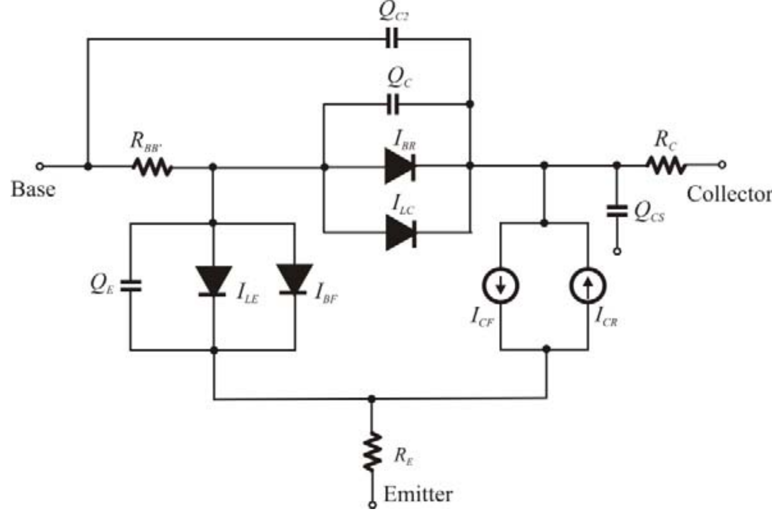


Figure 5.16 Large-signal model of BJT

The first two terms of equation (5.11) are related to the collector current flowing when each of the BE and BC junctions are forward-biased; each divided by their respective current gain β_F and β_R. The last two terms represent the current by the space charge region diode which is independent of the collector current.

It can be seen that the current due to the BE and BC junction diodes constitute the total collector current I_{CT}. The current is caused by two modes. That is, when the BE junction is forward-biased and the BC junction is reverse-biased (active mode); and the other when the BC junction is forward-biased and the BE junction is reverse-biased (inverse mode). In this case, since the current is in the reverse direction, it can be expressed as follows:

$$I_{CT} = \frac{I_S}{q_b}\left(e^{\frac{qV_{BE}}{n_F kT}} - 1\right) - \frac{I_S}{q_b}\left(e^{\frac{qV_{BC}}{n_F kT}} - 1\right) \quad (5.12)$$

The q_b in this expression is a factor representing the Early effect and the Kirk effect appearing in a large collector current and is expressed as follows:

$$q_b = \frac{1}{1 - \frac{V_{BC}}{V_A} - \frac{V_{BE}}{V_B}}\left(1 + \sqrt{1 + 4q_2}\right) \quad (5.13)$$

$$q_2 = \frac{I_S}{I_{KF}}\left(e^{\frac{qV_{BE}}{kT}} - 1\right) + \frac{I_S}{I_{KR}}\left(e^{\frac{qV_{BC}}{kT}} - 1\right) \quad (5.14)$$

V_A and V_B in equation (5.13) represent the forward and reverse Early voltages respectively while I_{KF} and I_{KR} represent the forward and reverse knee-currents of the collector current. The above represents an expression for the DC characteristics of the BJT. Figure 5.17 illustrates how these parameters are determined. Plotting I_B and I_C with respect to V_{BE} enables to extract the BE junction related parameters given by equations from (5.11) to (5.14). This is usually called *Gummel plot*. From Fig. 5.17, the knee-current of the collector current can be determined from the turning point and the slopes where the current shows saturation in a large collector current. For the base current on the other hand, the space charge region diode and the BE-junction parameters can be determined from the turning point and the slopes in a small base current. Similarly plotting the Gummel plot for V_{BC}, the BC-junction related parameters can be extracted. The parameters are grouped and shown in Table 5.1.

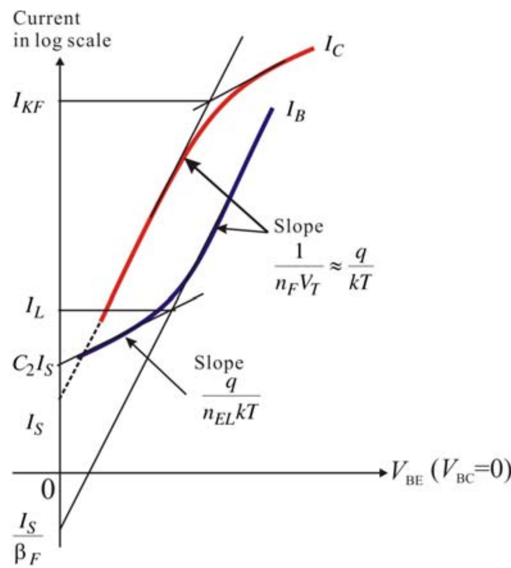


Figure 5.17 Gummel plot

Next, we consider the resistances caused by contacts. These are R_E, R_B and R_C; but of these, R_B is not a simple contact resistance. It varies according to the current, and two additional parameters (*RBM*, *IRB*) are thus required to describe it. These parameters are summarized in Table 5.1, and are classified as groups.

In addition, depletion and diffusion capacitances appear at the BE- and BC-junctions. The depletion capacitance having the parameters $C_{je}(0)$, the capacitance at 0 V, m_E the grading coefficient, and ϕ_{BE} the built-in potential is given by:

$$C_{JE} = \frac{C_{je}(0)}{\left(1 - \frac{V_{BE}}{\phi_{BE}}\right)^{m_E}} \tag{5.15}$$

The BE junction depletion capacitance parameters can be determined experimentally from C-V measurement for V_{BE}. Through curve fitting of the measured results with the equation given in (5.15), the parameters can be determined. Similarly, the same parameter group can be defined for the BC-junction depletion capacitance and the parameters BC-junction depletion capacitance can be

experimentally extracted using C-V measurement for V_{BC}. The parameters for the BE- and BC-depletion capacitances are also grouped and shown in Table 5.1.

However, because these BE- and BC- junction depletion capacitance expressions have singularity at $V_{BE}=\phi_{BE}$ and $V_{BC}=\phi_{BC}$, their application are usually limited to $V_{BE}\leq FC\cdot\phi_{BE}$ and $V_{BC}\leq FC\cdot\phi_{BC}$. For V_{BE} or V_{BC} values greater than these, a straight line that is given by the tangent at $FC\cdot\phi_{BE}$ is used instead of equation (5.15). Thus, the value *FC* in Table 5.1 represents the range of V_{BE} and V_{BC}.

Table 5.1 Gummel Poon model parameters

Parameter	Meaning	Parameter	Meaning
IS	Transport saturation current	NR	Reverse ideality factor
NF	Forward Ideality Factor	IKR	Reverse knee current
IKF	Forward knee current	NC	B-C ideality factor
NE	B-E ideality factor	ISC	B-C Saturation current
ISE	Base emitter saturation current	BR	Reverse beta
BF	Forward beta	VAR	Reverse Early voltage
VAF	Forward Early Voltage		
RE	Emitter resistance		
RC	Collector resistance		
RB	Zero bias resistance		
RBM	Minimum base resistance		
IRB	Current where base resistance half way between RB and RBM		
CJE	B-E Zero bias capacitance	CJC	B-C Zero bias capacitance
VJE	B-E Built-in potential	VJC	B-C Built-in potential
MJE	B-E grading coefficient	MJC	B-C grading coefficient
FC	Models transition from Junction to Diffusion capacitance		
XCJC	Models distributed nature of base		
TF	Forward transit time	TR	Reverse Transit time
ITF	Models TF dependence in ic		
VTF	Models TF dependence on Vbc		
PTF	Excess phase of TF		
XTF	Coefficient of TF bias dependence		

The diffusion capacitance is usually characterized by the transit time which appears in the active and inverse mode operations. Rather than the diffusion capacitance, the transit time is used and is represented by *TF* and *TR* in Table 5.1, respectively. In addition, since the transit time is not constant but depends on several parameters, the parameters that represent this dependence (*ITF*, *VTF*, *PTF*, and *XTF*) form a group. The capacitors Q_E and Q_C of Fig. 5.16 represent the capacitances due to the previously explained depletion and diffusion capacitances. The capacitor Q_{C2} and Q_{CS} depend on the fabrication method, and the reader may refer to reference [7] for details.

Also, a few more circuit elements can be added to the BJT equivalent circuit described in this book according to the fabrication process. The reader may again refer to other references for details.

5.2.3 Simplified Equivalent Circuit and S-parameters

Figure 5.18 shows a BJT small signal equivalent circuit derived from the large signal model in Fig. 5.16. Since the BC-junction is generally reverse-biased in active mode, the BC-junction can be represented by the parallel *RC* circuit. The value of g_μ is come from a reverse-biased diode and its value generally quite small. The capacitor C_μ represents a depletion capacitance. Similarly, the forward-biased BE junction can also be represented by the parallel RC circuit. The resistor g_π represents the small signal conductance of the forward biased diode. Note that the capacitor C_π represents the combined capacitances from the diffusion and depletion capacitances. Generally the diffusion capacitance is larger than the depletion capacitance and the value of C_π is mainly determined by the diffusion capacitance. In low-frequency application, diffusion capacitance C_π is typically small compared to g_π and so is neglected. However, in high frequency, C_π becomes dominant and the effects of both elements appear. Especially, in microwave, the occurrence of g_π can be neglected compared to C_π. Trans-conductance g_m represents the collector current controlled by the BE-junction voltage current source while g_c represents the resistance from the Early effect. Resistors R_E, R_B, and R_C represent the contact resistances.

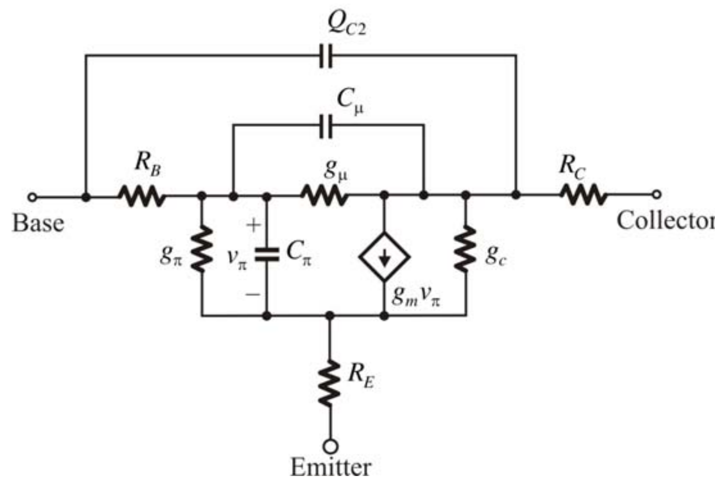


Figure 5.18 A small-signal equivalent circuit

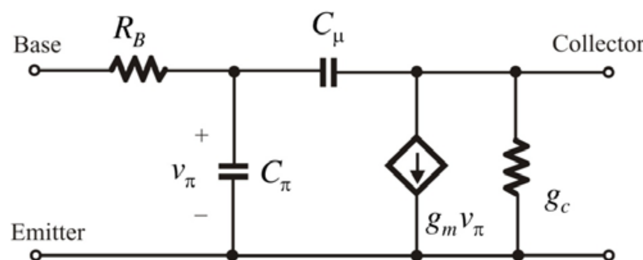


Figure 5.19 Simplified small-signal equivalent circuit

This circuit in Fig. 5.18 is complex and presents difficulty for qualitative understanding. Therefore, the simplified equivalent circuit of Fig. 5.19 is often used to explain qualitatively the measured S-parameters. The resistor g_π in the simplified equivalent circuit is ignored assuming high frequency application. Since the value of g_μ is also small, it is ignored and even C_μ is sometimes also often ignored. The values of R_E and R_C are typically small, and because they are the resistances caused by contacts, they are also ignored. The equivalent circuit thus obtained is as shown in Fig. 5.19.

In Fig. 5.20, similar to the FET, S_{11} and S_{22} are plotted on the Smith chart since they are related to impedance. On the contrary, S_{12} and S_{21} are the transfer functions and so are plotted on the polar chart showing their magnitude and phase. The magnitude of S_{21} is 10.0; i.e. the radial scale corresponds to a division of 2.0 per grid. On the other hand, as S_{12} is small, the radial scale is selected to be 0.2 per grid.

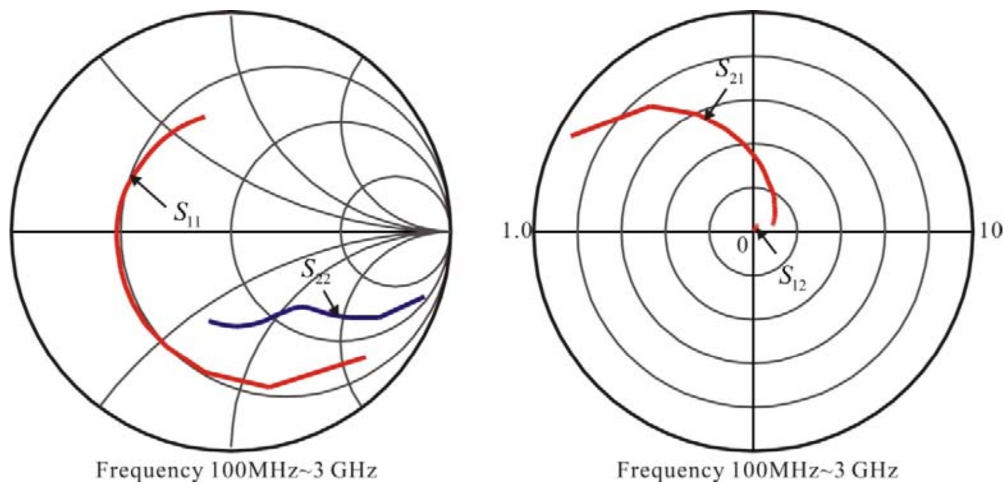


Figure 5.20 Measured S-parameters of BJT

Here, the input impedance includes the bonding wire in the measurement. Thus, the input becomes approximately a series *RLC* circuit from the simplified equivalent circuit shown in Fig. 5.19. Thus, the locus of the S-parameters follows a constant resistance circle as shown in Fig. 5.20. At low frequency, the locus lies in the capacitive region of the Smith chart. On the other hand, as the frequency increases, the inductance of the bonding wire becomes dominant and so the locus lies in the inductive region. Then the resistance value in the simplified equivalent circuit is found to approximately correspond to the base resistance R_B. In addition, by using the method described in Chapter 2 and computing the *L* and *C* values at resonance, the inductance and capacitance of the bonding wire can be obtained respectively. The obtained capacitance can be interpreted as C_π.

In the case of S_{22}, because the collector resistance g_c is small, the effect of g_c is seldom observed in S_{22}. Rather than g_c, the output circuit can be approximated as the series connection of C_μ and $r_\pi \|$ (Z_o+R_B) for extremely low frequency. In this case, because r_π is generally big, the output circuit appears to be approximately the series connection of C_μ and (Z_o+R_B). Therefore, the locus moves following the constant resistance circle. As the frequency becomes higher, the approximate output circuit appears to be g_c in parallel with a parasitic capacitor C_c. Thus, with increasing frequency, the locus moves along the constant conductance circle. Due to the effect of C_c, the trajectory appears in

the capacitive region. The resulting locus is the combined locus; that moves along the constant resistance circle in low frequencies, and moves along the constant conductance circle in high frequencies. Even though not shown here, with further increase in frequency, the trajectory of S_{22} follows that similar to S_{11} due to the effects of bond wire inductors and C_μ.

From the simplified equivalent circuit of Fig. 5.19, the magnitude and phase of S_{21} is

$$S_{21} = -2g_m Z_o = 2g_m Z_o \angle 180° \tag{5.16}$$

Therefore, by using the low frequency measurement data, the approximate value of g_m can be determined. Since the voltage across C_π decreases as the frequency increase, its magnitude decreases. It can also be seen that the phase increases in clockwise direction. Similar to the FET explanation, we also can see that for low frequency limit S_{12} becomes

$$S_{12} = 2j\omega C_\mu Z_o = 2\omega C_\mu Z_o \angle 90° \tag{5.17}$$

and with increasing frequency, the phase of S_{12} can also be seen to increase in clockwise direction. From the above equation, it can be found that the magnitude also increases as the frequency increases.

5.2.4 Package

Figure 5.21 shows a typical example of a low power BJT package. In Fig. 5.21, the BJT is first attached to the lead-frame. It is worth noting that, the bottom of the chip generally becomes the collector (from Fig. 5.13(b)). Then each of the terminals is wire-bonded to the corresponding terminals. Since the parasitic elements from the assembly of the emitter terminal provide feedback from output to input, they have a significant impact on device performance. In order to minimize these parasitic emitter inductances appearing through the assembly, it is common to assign two terminals to the emitter.

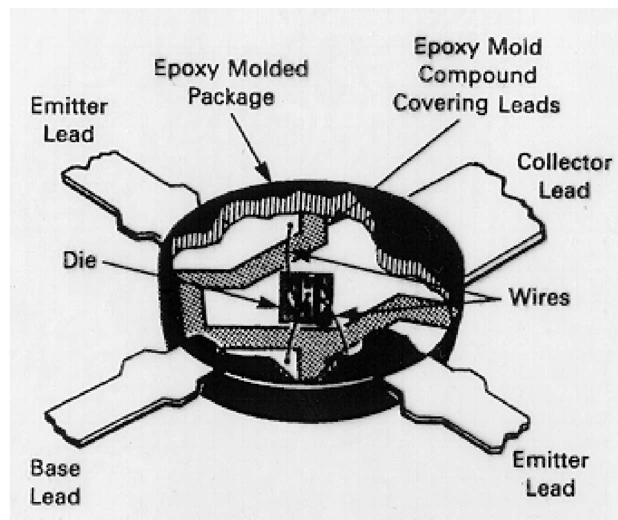


Figure 5.21 Example of low power BJT package

After such an assembly, molding is done around the wire bonded chip using epoxy material. Then, the lead terminals are appropriately cut from the lead-frame to be used as a packaged device. Such packaging for BJT will result in performance degradation at high frequencies as in the case of FET.

5.2.5 GaAs/AlGaAs HBT

Figure 5.22 shows the cross-sectional structure of a GaAs Hetero-junction Bipolar Transistor (HBT). The advantages of compound semiconductor GaAs over Si and the characteristics of hetero-junction are employed in the GaAs HBT to improve the performance of Si BJT. However, note that the base and emitter has the same structure of the interdigital finger type as in Si BJT

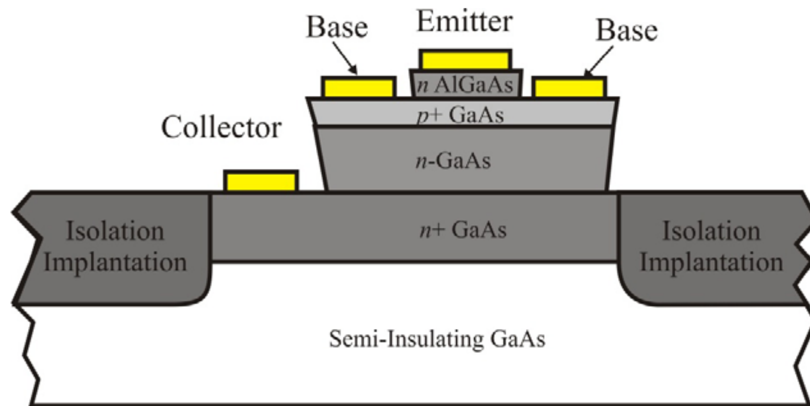


Figure 5.22 Cross-sectional structure of GaAs HBT

The BE-junction of the GaAs HBT is formed by using an *n*-type AlGaAs in the emitter and p-type GaAs in the base. Thus, an energy trap occurs between the AlGaAs and GaAs hetero-junction. The energy trap is useful to suppress the diffusing holes from the base toward the emitter which appears for a forward-biased BE-junction. The diffusing holes are easily trapped and therefore the hole diffusion is significantly suppressed. Due to the energy trap, the doping of the base region can be increased. As a result, the base resistance at high frequencies which limits device performance can be made smaller. Therefore, the unit gain frequency given by the following equation is increased.

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_\mu}} \tag{5.18}$$

Here f_T is the cut-off frequency where the short circuit current gain becomes unity. The frequency $f_{\max}$ represents the maximum oscillation frequency where the maximum power gain becomes unity.

As previously explained, the injected electrons from the emitter to the base arrive at the collector by diffusion. Thus, the base transit time τ_b is determined by the diffusion constant. The diffusion constant of electrons in GaAs, D_n is four times bigger compared to that in Si, and the

smaller base transit time results. Such base transit time τ_b is directly related cutoff frequency f_T. This results in further increase in $f_{\max}$ given by (5.18).

The electrons arrived at the collector then move the collector region by drift mechanism and finally reach to the collector terminal. Assume that the devices having the same collector thickness fabricated using Si and GaAs. The drift velocity of electrons in GaAs, v_d is approximately six times faster than in Si. As a result, this will reduce the collector transit time, τ_d. This also leads to a rise in f_T. Thus, GaAs HBT can be used up to 10 GHz, due to such improvements and with more advanced processes it can be used up to the millimeter wave frequency.

5.3 DC BIAS CIRCUIT

In order to use BJT or FET as an amplifier or oscillator, it is common to apply an appropriate DC voltage. Such DC bias circuit is similar to that in low frequency amplifier design in that, the DC bias circuit sets the operating point of nonlinear device, but the structure of the DC bias circuit for RF transistors differs slightly from that of the low frequency. The DC bias circuit must not affect the RF signal flow and decoupling of the bias circuit is necessary to achieve this. In this section, the application of DC voltage to RF transistors as well as decoupling method will be discussed.

5.3.1 BJT DC Bias Circuit Design

5.3.1.1 DC Bias Circuit

Figure 5.23 shows two typical methods of biasing BJT.

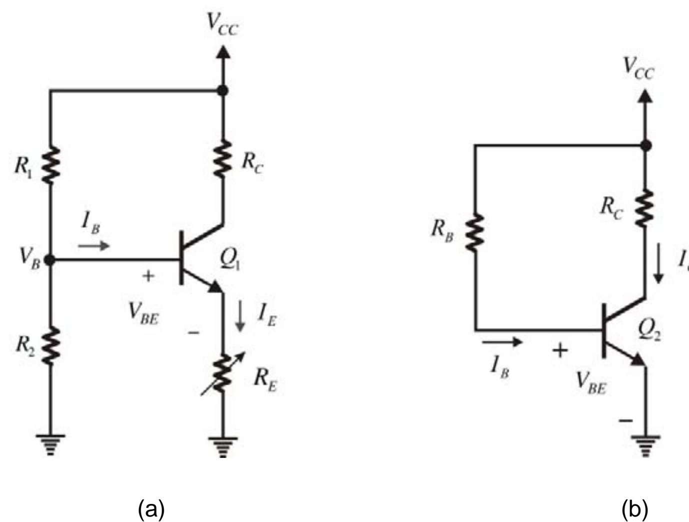


Figure 5.23 DC bias circuit; (a) using emitter resistor, (b) emitter resistor removed

Consider Fig. 5.23(a); neglecting the base current, the supply voltage V_{CC} divided by resistors R_1 and R_2 appears at the base. The base voltage V_B is

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}, \tag{5.19}$$

and the emitter current I_E is determined as

$$I_E = \frac{V_B - V_{BE}}{R_E} \quad . \tag{5.20}$$

Thus, the desired emitter current is obtained by varying resistor R_E. In addition, since the RF output is usually taken from the collector, the voltage V_{CE} will be limited by resistor R_C. In order to overcome this RF signal swing limitation, RF choke (RFC) is often used instead of resistor R_C.

In the case of Fig. 5.23(b), the base current is obtained as follows:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}. \tag{5.21}$$

Thus, the collector current is subsequently given by

$$I_C = \beta I_B. \tag{5.22}$$

The value of β is generally wide spread. This makes the collector current determined by (5.22) also wide spread, and the current may generally different from design value. When using this DC bias circuit, consequently the need to adjust the resistance R_B in order to obtain the desired collector current arises. On the contrary, the bias circuit using emitter resistor yield a stable designed collector current. Therefore, the DC bias circuit of Fig. 5.23(b) is not generally used at low frequencies, and the circuit in Fig. 5.23(a) is preferred.

However, the emitter terminal is usually grounded in RF application, and a stable ground is needed for RF application. When the bypass capacitor is added in parallel to the emitter resistor R_E in Fig. 5.23(a) for AC ground, many problems arise due to unstable AC ground. Practically, such configuration is accompanied by unpredictable small parasitic elements between the emitter terminal and the ground. Even, assuming an ideal bypass capacitor, in order to connect it in parallel with the resistance R_E, it must inevitably require some landing patterns and connection lines which make it very difficult to correctly predict the impedance attached to the emitter terminal. In worst situations, the parasitic impedance at the emitter may cause oscillations, or may even significantly change the optimum RF matching impedance, which often leads to failure in obtaining the desired gain. Thus, although the circuit of Fig. 5.23(a) supplies a stable DC collector current, this type of DC bias circuit is avoided especially in the case of packaged transistors due to the problems in RF operation. On the other hand, despite the flaws of the bias circuit of Fig. 5.23(b), such as, the device-to-device DC collector current change and the necessity of the adjustment of R_B, the circuit is preferred in RF application because it provides a stable RF ground.

5.3.1.2 RF Decoupling

Figure 5.24 shows an example of the decoupling of a designed DC-bias circuit from RF circuit. The two capacitors C_B blocks the DC current flowing out through RF input and output and are called as DC block capacitor. The capacitor is usually sufficiently set large to behave as a short at the operating frequency. However, such DC block capacitors are not pure capacitors. As described in Chapter 2, parasitic elements such as series inductor are inherent in the capacitors. As a result, a

large valued chip capacitor may not function as a DC block at higher operating frequency and can often cause significant insertion loss due to the parasitic series inductor. In general, up to a frequency of a few hundred MHz, the chip capacitor operates well as a DC block because the value of the series inductor is small. However beyond this frequency range, the capacitor does not work well as a DC block due to the influence of the series inductor. Such capacitors should be replaced by other capacitors to behave as a true DC block. In the case of thin film implementation, MIM capacitors can be also used for truer DC block. The MIM capacitors can be usually connected through a wire bonding. Since the bonding wires yield inductances also, the length and number of bonding wires should be set to accompany minimal parasitic inductances. In PCB assembly, the DC block is often constructed with coupled transmission lines. However the coupled lines can be used usually as a narrowband DC block. Thus they can be used in the case that a broadband operating DC block is not required. Using coupled line DC block, the effect of the imprecise parasitic inductances occurring during circuit construction is minimized.

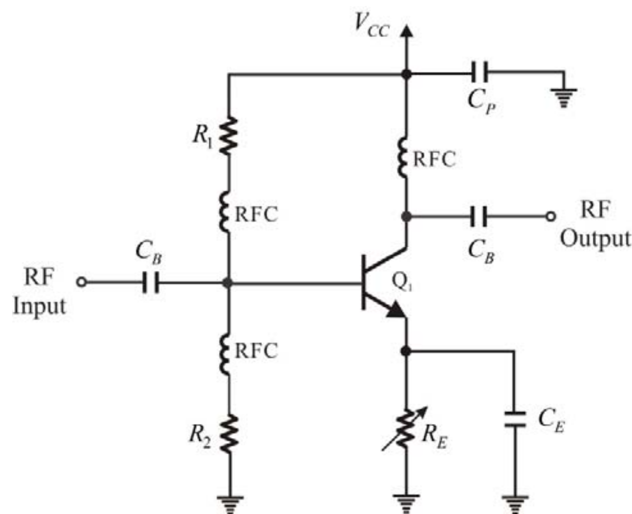


Figure 5.24 RF decoupled circuit example

The next problem is the selection of bypass capacitors C_E for providing the RF ground and the bypass capacitor C_P for isolating the RF circuit from the external bias circuitry. The bypasses capacitor C_P, similar to the DC block capacitor, must be selected to be sufficiently large to behave as a short at the operating frequency. It is necessary that C_P must be placed not to affect the RF circuit. Its effect must be carefully considered in advance whether the flow of RF signal could be affected. Obviously, when C_P is sufficiently large, the lower frequency AC noise from DC supply which may flow into the internal RF circuitry can be effectively blocked. However, such capacitors do not act as a short at RF as discussed in DC block. Thus, to prevent this, two parallel capacitors or sometimes *multiple capacitors in parallel* are often used. In this case, a small-value capacitor operating as a short at RF and a large valued capacitor to take care of the AC noise of DC supply.

In addition, the capacitor C_E is inserted to provide RF ground. Since capacitor C_E bypasses the emitter resistor, it is called also bypass capacitor. However such bypass capacitor causes a lot of problems at high frequencies. It must necessarily be chosen so that it is a short at RF. Besides, for the effect of possible extra connecting lines such as landing patterns should be minimized. This effect is more pronounced as the operation frequency becomes higher and so it is usually not

recommended, except for oscillators and for amplifiers operating at frequencies below a few hundred MHz.

The RFC (RF choke) of Fig. 5.24 acts as an open-circuit at the operating frequency and makes the collector terminal to be open. In the case of RFCs connected to the base, they make the base terminal open from the bias resistors. In general however, the RFC bandwidth is narrow and other resonance phenomena are expected. *RFCs are not necessary where a resistor can sufficiently ensure an open-circuit for RF*.

Thus, for the base side of Fig. 5.24, if the objective can be achieved using resistors, it is generally a good idea to use resistors alone without the addition of RFCs due to the broadband characteristics of resistors. In case of collector resistor usage, a resistor cannot be used because the DC current flows in the collector side. So it is necessary to use RFC in spite of resonance and the narrow band property. In this case, the RFC is selected to resonate at the frequency of operation since it appears as open. It is recommended to have RFC operate near such resonance point in the selection.

5.3.1.3 Active DC Bias Circuit

Figure 5.25 shows an active DC bias circuit. Transistor Q_1 is a DC biasing low frequency operating *pnp* transistor and transistor Q_2 represents RF transistor.

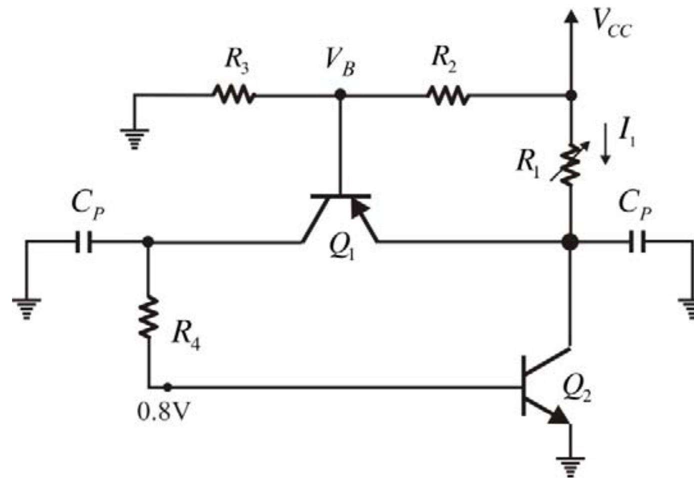


Figure 5.25 An active DC bias circuit

Regarding the operation of this circuit, the voltage V_{CC} divided by resistors R_2 and R_3 appears at the base of Q_1. Thus, base voltage V_B of Q_1 becomes

$$V_B = \frac{R_3}{R_2 + R_3} V_{CC} . \tag{5.23}$$

Therefore, a current

$$I_1 = \frac{V_B - V_{BE}}{R_1} . \tag{5.24}$$

will flow through resistor R_1 and this current is the sum of the collector current of Q_2 and the emitter current of Q_1.

The emitter current of Q_1 becomes the base current of Q_2, which is negligible compared to the collector current of Q_2. Thus, I_1 approximately becomes the collector current of Q_2. Therefore it can be seen that, the current flowing in the transistor Q_2 is determined by the resistor R_1 as in (5.24) regardless of the β of the transistor. Note that the emitter of transistor Q_2 is also directly grounded, and the circuit is found to retain the two advantages of DC bias circuits in Fig. 5.23. The disadvantage is that, the supply voltage V_{CC} must be greater than the collector voltage of transistor Q_2. This becomes a serious problem when the collector current is large because the power loss due to the collector resistor R_1 becomes high. The bypass capacitors shown in the figure can be used to isolate the DC bias circuit and the RF. The selection of such capacitors is the same as the selection of the bypass capacitor C_P previously described.

5.3.2 FET DC Bias Circuit Design

The unique thing about the DC bias circuit for a depletion mode FET is that a negative voltage is necessary for the gate bias. Figure 5.26 shows two types of DC-bias circuit for the depletion mode FET.

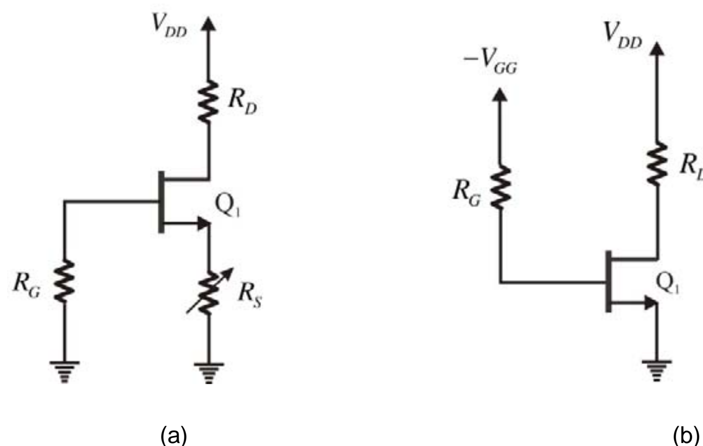


Figure 5.26 FET DC bias circuit: (a) Self bias circuit, (b) DC bias circuit using two DC sources

In Fig. 5.26(a), source resistor R_S is inserted. So when the drain current flows, a voltage drop across the resistor R_S appears. However, since current does not flow through the gate, the gate DC voltage is 0. Therefore the voltage across resistor R_S is developed in a negative direction between gate-source. This gate-source voltage determines the drain current and the drain current can be adjusted by adjusting the resistor R_S. If resistor R_S is chosen to be a large value, a large reverse voltage across the gate-source appears and the drain current becomes small. On the other hand, when R_S is small, a large drain current flows. Since there is usually no current flowing in the gate, the gate resistor R_G has no effect. The reason for inserting the gate resistor in this circuit is for the protection of the device. In abnormal operation, a positive voltage may appear across the gate and large current flows which may damage the FET. To prevent such situations, a resistor is often inserted in the gate for protection. This circuit is called a self-bias circuit.

In the case of Fig. 5.26(b), two DC voltage sources are used. A negative DC voltage applied to the gate while a positive voltage is applied to the drain. Thus, drain current is adjusted by the voltage $-V_{GG}$. The reason for inserting the resistor R_G in the gate is the same as for Fig. 5.26(a). The resistor inserted in the drain is to set the drain-source DC voltage. This resistor may not be needed depending on the situation. Furthermore, these two circuit operations are the same as those for BJT DC bias circuits. Figure 5.26(a) gives a stable DC drain current while Fig. 5.26(b) gives a stable RF ground.

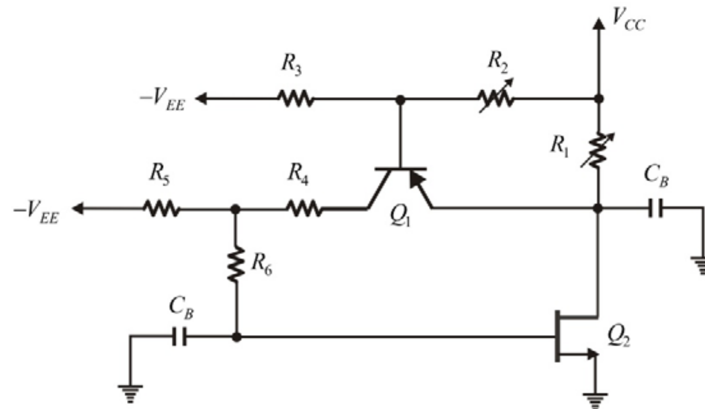


Figure 5.27 Active DC bias circuit

Figure 5.27 shows an active DC bias circuit of FET. The transistor Q_1 is a low-frequency biasing *pnp* transistor while Q_2 represents an RF FET. Resistors R2 and R3, like in the case of BJT active DC bias circuit, are for the division of the supply voltage. The difference being that, both negative and positive voltages are used in the FET. Based on the voltage division, the current determined by resistor R_1 flows through transistors Q_1 and Q_2, and the most of the emitter current of Q_1 appears at the collector. The negative voltage as a result of the voltage division appears at the gate of the FET which determines the DC current flowing in the drain of the FET. The method of isolating the DC bias circuit is similar to the case of the BJT. Also, the resistor R_6 inserted in the gate is intended to protect the FET from being damaged when large current flows as a result of possible positive voltage appearing at the gate in abnormal operation.

5.3.3 S-parameter Simulation

Figure 5.28 shows an S-parameter simulation example for a FET. The same concept can be used for real measurement using test equipments. The DCFEED in Fig. 5.28 is a component representing an RFC which becomes a short for DC and an open for RF. The DC block represents a component that is open at DC and short for all RF frequencies. The gate and drain voltages are set to V_{GS}=–1 and V_{DS}=3. Note that bypass capacitors for DC voltage supplies are not necessary because DC source is completely short-circuited to AC in ADS simulation.

Figure 5.29 shows the S-parameter simulation results. When S-parameter simulation is performed with such a set up, DC analysis will automatically be performed first without the need to separately specify it. At the established DC operating point, FET will be converted automatically into the corresponding small-signal equivalent circuit, and the S-parameters of the FET will be

computed and outputted. The computed S-parameters are found to show the frequency response previously explained.

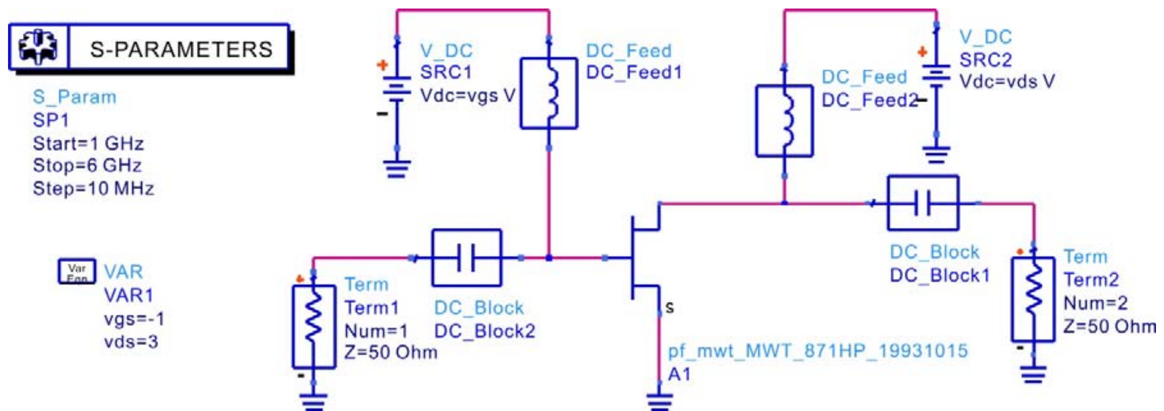


Figure 5.28 S-parameter simulation of FET

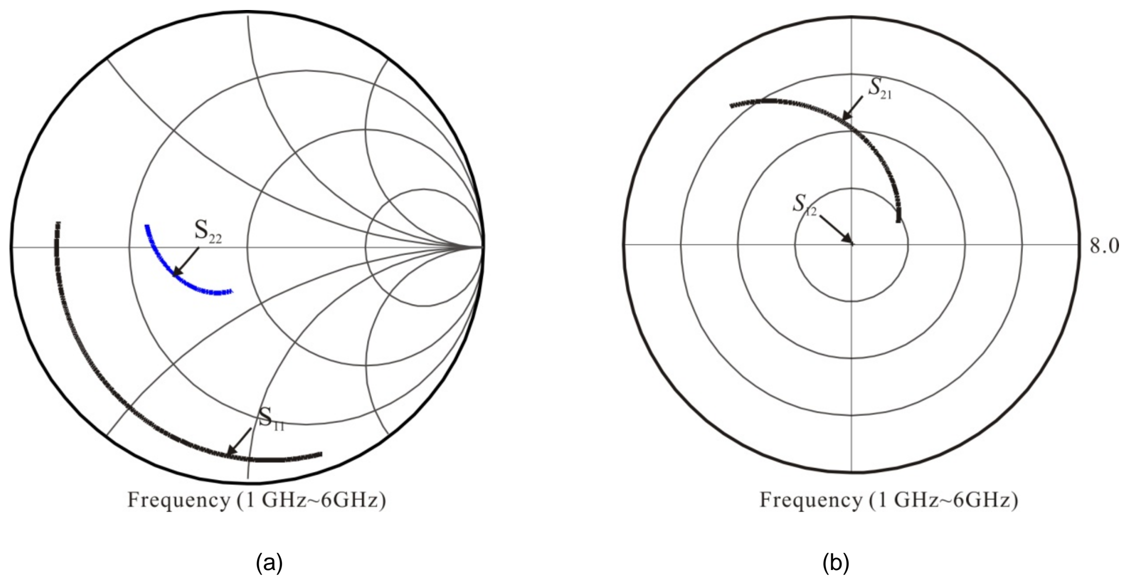


Figure 5.29 S-parameter simulation results: (a) S_{11} and S_{22}, (b) S_{21} and S_{12}

Figure 5.30 shows a BJT S-parameter simulation setup. It is similar to FET S-parameter simulation. The only difference is that a DC current source is used for DC biasing the base. Since the operating point of the BJT is usually determined by DC collector current, the corresponding base current is supplied by the current source. Furthermore, because the DC current source is open at AC, an RFC will not be needed. The calculated results of this set up are shown in Fig. 5.31.

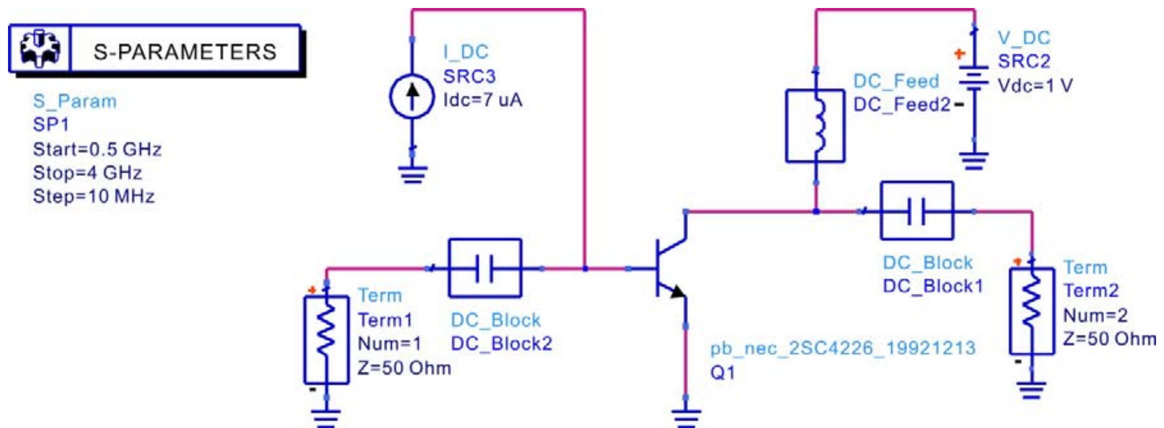


Figure 5.30 BJT S-parameter simulation setup

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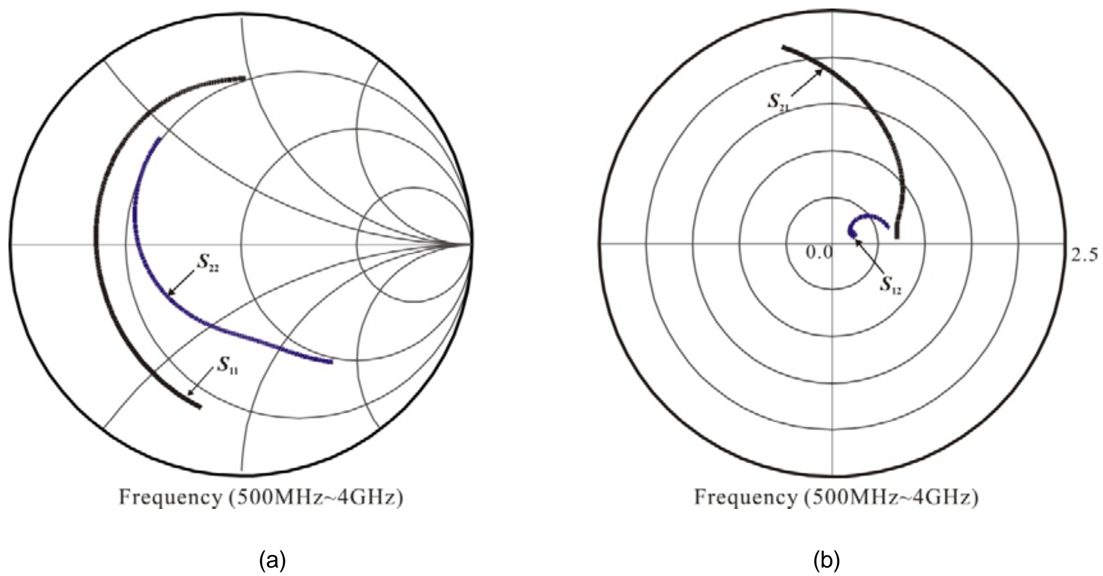


Figure 5.31 S-parameter simulation results: (a) S_{11} and S_{22}, (b) S_{21} and S_{12}

5.4 EXTRACTION OF FET SMALL-SIGNAL EQUIVALENT CIRCUIT

Rather than S-parameter itself, a physical equivalent circuit for a microwave passive or active device sometimes gives more insight to designers and provides a way to understand the operation of a device. In addition, many microwave devices can be represented as either T-type or Pi-type equivalent circuit. Therefore, the values of the equivalent circuit elements often need to be extracted from the measured S-parameters for further analysis and design. For devices that can be represented by T- and Pi equivalent circuits, the extraction of the values can easily be carried out by converting the S-parameters to Z- and Y-parameters. Since the Z- and Y-parameters themselves can be

naturally represented as T-type or Pi- type circuits respectively, the values of T- and Pi type equivalent circuits can then be easily obtained using the converted Z- or Y-parameters.

Figure 5.32 shows a T-type equivalent circuit. Now we will show that the derivation of the T-type equivalent circuit from the Z-parameters converted from the measured S-parameters. From the definition of Z-parameters, the port voltages can be expressed as follows:

$$V_1 = z_{11} I_1 + z_{12} I_2 . \tag{5.25}$$

$$V_2 = z_{21} I_1 + z_{22} I_2 . \tag{5.26}$$

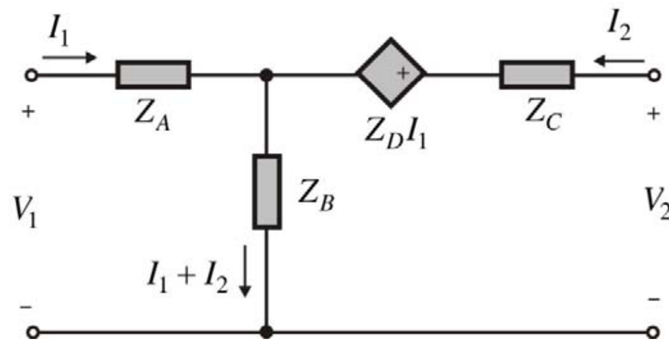


Figure 5.32 T-type equivalent circuit

Since voltage V_1 at port 1 depends on the current I_1 and I_1+I_2, transforming equation (5.25),

$$V_1 = \left(z_{11} - z_{12} \right) I_1 + z_{12} \left(I_1 + I_2 \right) . \tag{5.27}$$

Then, Z_A and Z_B become

$$Z_A = z_{11} - z_{12} , \tag{5.28}$$

$$Z_B = z_{12} . \tag{5.29}$$

Also, arranging voltage V_2 at port 2 in terms of I_2 and I_1+I_2, and arranging the remaining terms in terms of current I_1, we obtain

$$V_2 = z_{21} I_1 + z_{22} I_2 = z_{12} \left(I_1 + I_2 \right) + \left(z_{22} - z_{12} \right) I_2 + \left(z_{21} - z_{12} \right) I_1$$

Comparing the above equation with the circuit in Fig. 5.32, yields

$$Z_C = z_{22} - z_{12} , \tag{5.30}$$

$$Z_D = z_{21} - z_{12} . \tag{5.31}$$

Using results from (5.28) to (5.31), the circuit in Fig. 5.32 can be represented as shown in Fig. 5.33. Multi-port Z-parameters can also be expressed in a similar way, and this is used to model discontinuity effects which mainly appear in waveguide [8].

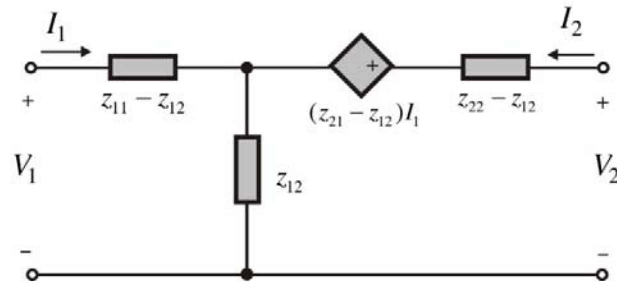


Figure 5.33 Z-parameter equivalent circuit

Similarly, Y-parameters can be represented by a Pi-type equivalent circuit. Figure 5.34 shows the Pi-type equivalent circuit. Note that when two port voltages are simultaneously present, the current flowing from port 1 to port 2 depends on the voltage V_1–V_2. Using this, the port 1 current can be expressed as follows;

$$I_1 = y_{11}V_1 + y_{12}V_2 = -y_{12}\left(V_1 - V_2\right) + \left(y_{11} + y_{12}\right)V_1$$

And the port 2 current can be expressed as,

$$I_2 = y_{21}V_1 + y_{22}V_2 = -y_{12}\left(V_2 - V_1\right) + \left(y_{22} + y_{12}\right)V_2 + \left(y_{21} - y_{12}\right)V_1$$

Analyzing these equations, it can be seen that these can be represented by the circuit shown in Fig. 5.34.

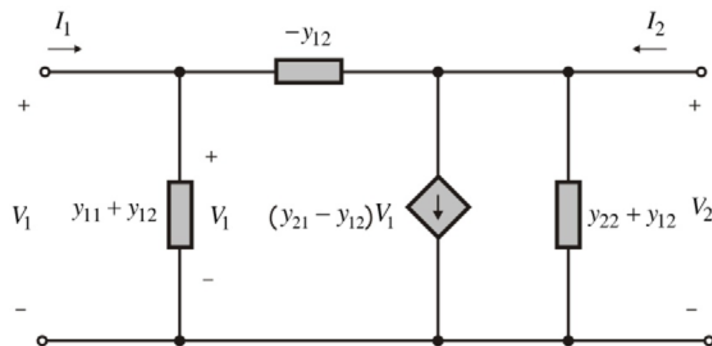


Figure 5.34 Pi-type equivalent circuit

Considering the circuits in Fig. 5.33 and Fig.5.34 for passive devices, they can be illustrated in a simplified form as shown in Figs. 5.35(a) and (b), respectively since by reciprocity z_{12}=z_{21} in Z-parameters and y_{12}=y_{21} in Y- parameters.

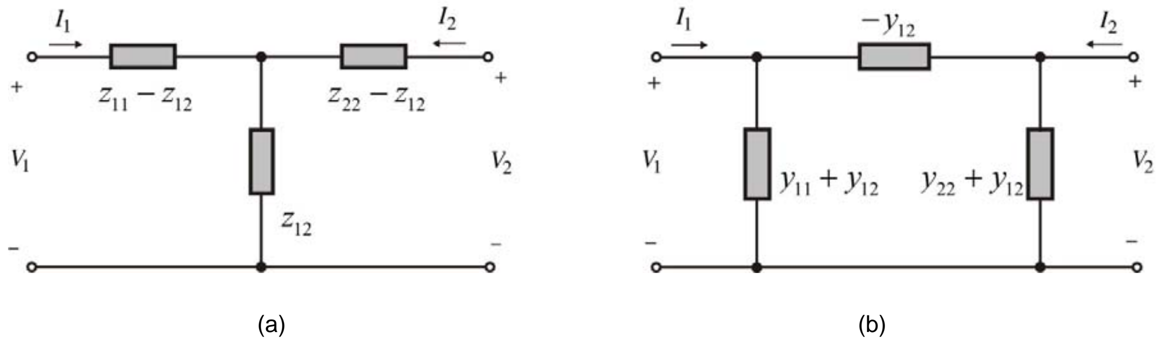


Figure 5.35 The equivalent circuit for a passive device (a) in Z-parameters (b) in Y-parameters

The circuits in Fig. 5.35 are useful for analyzing unknown inductor or capacitor using the Z- or Y-parameters. Practically, the values of the computed (z_{11}–z_{12}), z_{12}, and (z_{22}–z_{12}) in the T-type equivalent circuit, and those of (y_{11}–y_{12}), y_{12}, and (y_{22}–y_{12}) in the Pi-type equivalent circuit may not be represented by a single element such as inductor or capacitor, and may show a frequency dependence. In this case, the frequency dependence of each element can be decomposed and be represented by the complex circuit consists of the combination of series or parallel connection of frequency independent elements as explained in Chapter 2. In addition, using a similar technique, multi-port passive device can be represented in a similar way. The reader may refer to other references [8] for details.

■ Example 5.1

For a 10mil thick alumina substrate with a permittivity 9.6, the equivalent circuit of a microstrip ring type inductor which has 2 turn, width and spacing of 10mil, and inner radius of 50 mil can be represented by the circuit in Fig. 5E.1 for frequencies up to 2GHz. Calculate the values of the equivalent circuit. Here L_s represent the inductance arising from the microstrip ring type inductor and C_{p1} and C_{p2} represent the parasitic capacitances.

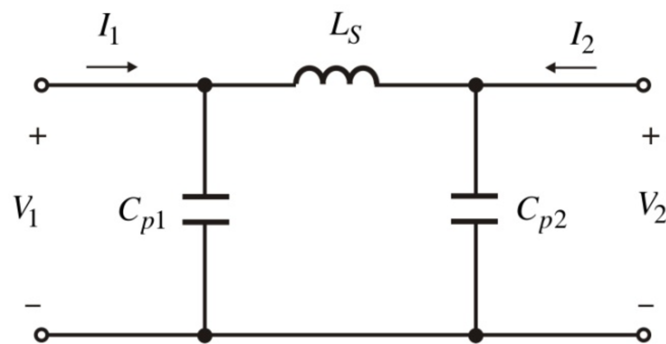


Figure 5E.1 Ring microstrip inductor equivalent circuit

Solution
Figure 5E.2 shows the set up for S-parameter simulation of the microstrip ring inductor.

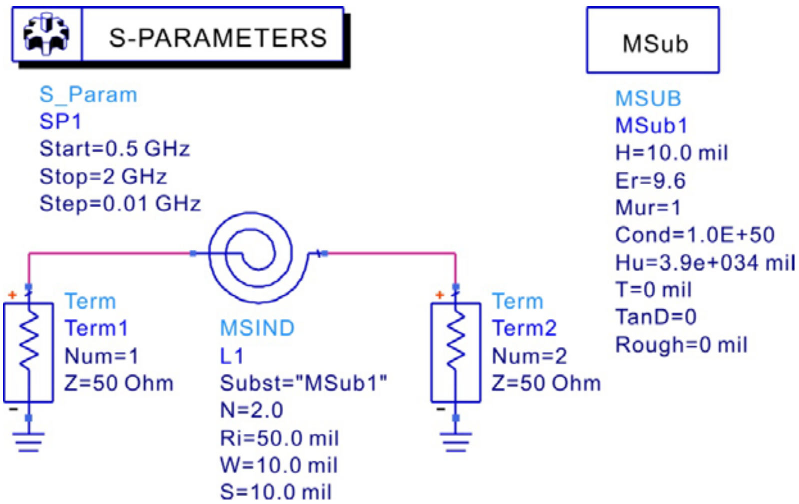


Figure 5E.2 S-parameter simulation of microstrip ring type inductor

Before calculating S-parameters, open the S-parameter simulation controller, and check the Y-parameter calculation in the **Parameters** tab. Such setting provides the S-parameters as well as the Y-parameters to be stored in the dataset after the simulation. The following equation shown in Fig. 5E.3 is then inserted in the Display window. If this is plotted with respect to the frequency, the result of Fig. 5E.4 can be obtained.

Eqn w=2*pi*freq

Eqn Cp1=(imag(Y(1,1)+Y(1,2)))/w

Eqn Cp2=(imag(Y(2,2)+Y(1,2)))/w

Eqn Ls=-1/imag(-Y(1,2))/w

Figure 5E.3 Equation for calculating the value of the equivalent circuit of Fig. 5E.1

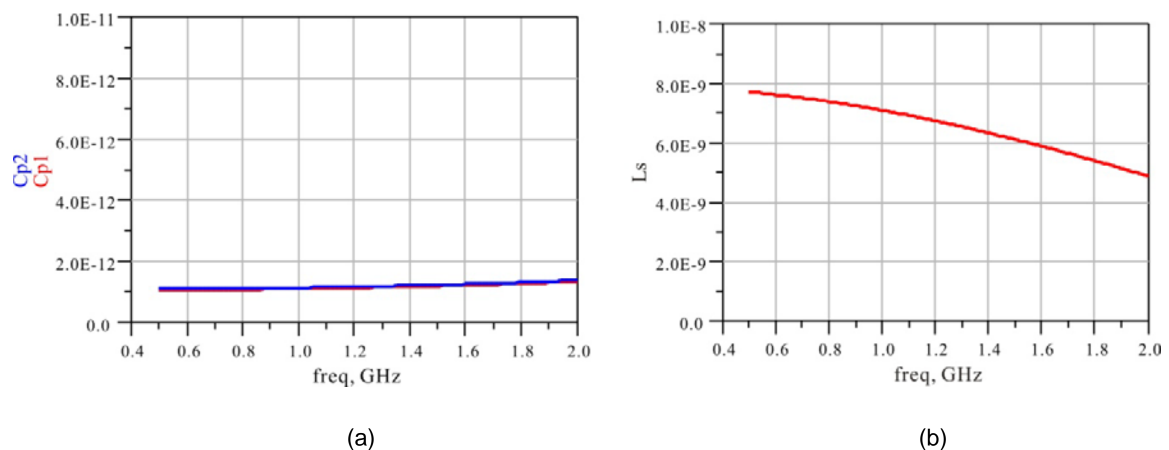


Figure 5E.4 (a) Capacitance **Cp**1 and **Cp**2 and (b) series inductance of ring microstrip inductor

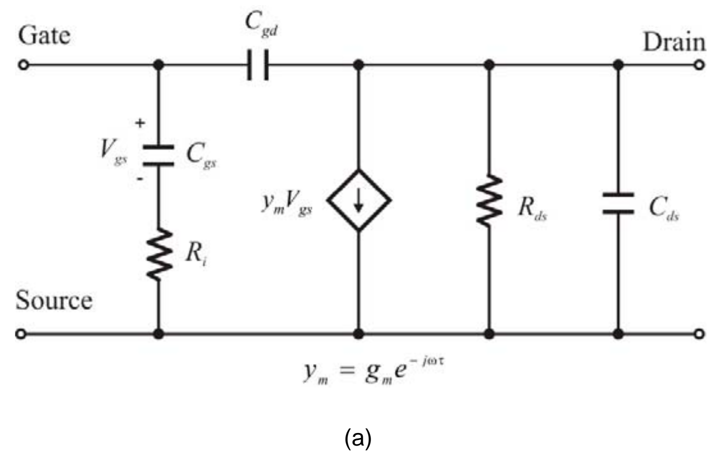
Cp1 in Fig. 5E.3 represents the shunt capacitor at port1 while **Cp**2 represents the shunt capacitor at port 2. Inductor, **Ls** represents the series inductor connecting port1 and port 2. Note that **Cp**1 and **Cp**2 are almost frequency independent. However, Ls shows some frequency dependence. Thus **Ls** cannot be represented by a simple inductor and should be represented by more complex circuit.

■

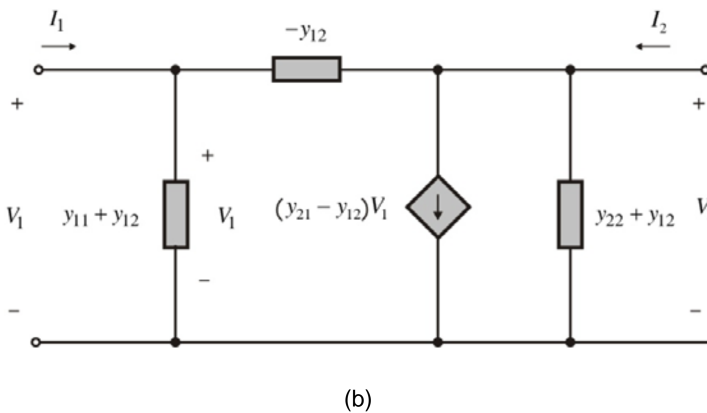
We now present the method of obtaining the values of the simplified equivalent circuit shown in Fig. 5.7 from measured S-parameters. The Pi-type equivalent circuit in Fig. 5.36(b) is similar to the simplified equivalent circuit of FET shown in Fig. 5.36(a). Therefore, by directly matching the simplified FET equivalent circuit to the Pi-type equivalent circuit, the values of such simplified equivalent circuit can be directly obtained from the measured S-parameters. First, considering the output impedance, the admittance of $R_{ds}||C_{ds}$ should be equal to $y_{22}+y_{12}$. Therefore, it can be seen that,

$$R_{ds}^{-1} = \mathrm{Re}\left(y_{22} + y_{12}\right), \tag{5.32}$$

$$C_{ds} = \frac{1}{\omega}\mathrm{Im}\left(y_{22} + y_{12}\right). \tag{5.33}$$



(a)



(b)

Figure 5.36 (a) GaAs FET simplified equivalent circuit and (b) Y-parameter equivalent circuit

Comparing y_{12} and C_{gd}, we obtain

$$C_{gd} = \frac{1}{\omega}\operatorname{Im}\left(-y_{12}\right). \tag{5.34}$$

From the comparison of the input impedances, we obtain

$$\frac{1}{y_{11}+y_{12}} = R_i + \frac{1}{j\omega C_{gs}}. \tag{5.35}$$

Using (5.35), R_i and C_{gs} can be determined as follows:

$$R_i = \operatorname{Re}\left(\frac{1}{y_{11}+y_{12}}\right), \tag{5.36}$$

$$\frac{1}{\omega C_{gs}} = -\operatorname{Im}\left(\frac{1}{y_{11}+y_{12}}\right). \tag{5.37}$$

The difference in the dependent-sources in Fig. 5.36(a) and (b) is the control voltage which in the case of (a) is the voltage V_{gs} across C_{gs} while in the case of Fig. 5.36(b), the control voltage is V_1. This requires some adjustment. The relationship between V_1 and V_{gs} is

$$\frac{V_{gs}}{V_1} = \frac{1}{1+j\omega C_{gs}R_i} = \frac{\operatorname{Im}\left(\frac{1}{y_{11}+y_{12}}\right)}{\frac{1}{y_{11}+y_{12}}}$$

Also, since

$$\left(y_{21}-y_{12}\right)V_1 = y_m V_{gs}$$

g_m is obtained as follows:

$$g_m = \left|y_{21}-y_{12}\right|\cdot\left|\frac{V_1}{V_{gs}}\right| = \frac{\left|y_{21}-y_{12}\right|}{\left|y_{11}+y_{12}\right|}\left\{\operatorname{Im}\left(\frac{1}{y_{11}+y_{12}}\right)\right\}^{-1}. \tag{5.38}$$

And τ is determined as

$$\tau = -\frac{1}{\omega}\angle\left(j\frac{y_{21}-y_{12}}{y_{11}+y_{12}}\right). \tag{5.39}$$

Therefore, the values of the simplified equivalent circuit of FET can be directly determined using the equations from (5.32) to (5.39)

■ Example 5.2

This example shows how to obtain the simplified FET equivalent circuit. Open the model of the chip pHEMT FHX15 in ADS library and extract the simplified FET equivalent circuit at V_{DS}=2V and V_{GS}=–0.2V

Solution

Figure 5E.5 shows a DC simulation setup. The I_D–V_{DS} characteristics are plotted in Fig. 5E.6. From this, the drain current can be found to be I_{DS}=18 mA.

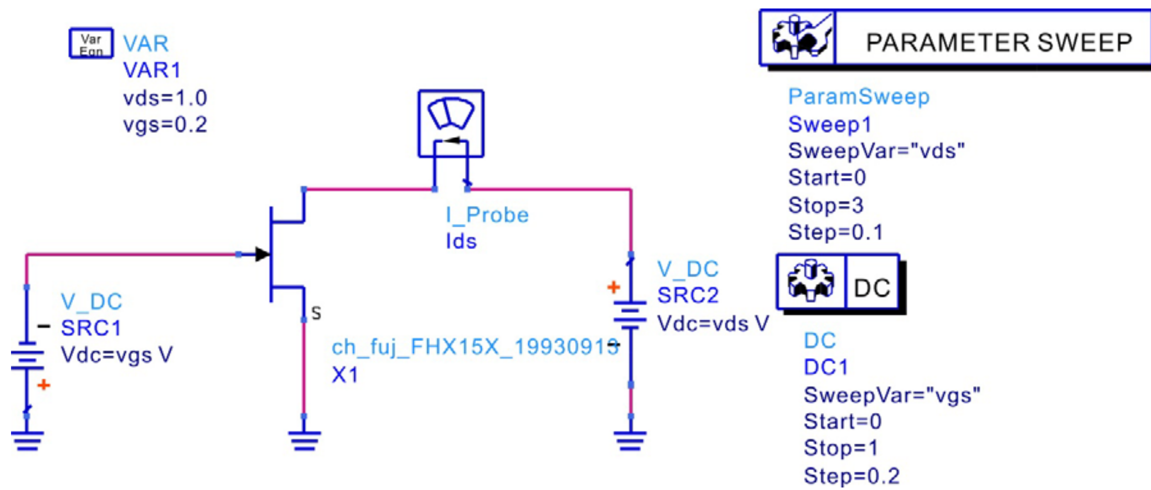


Figure 5E.5 DC simulation circuit

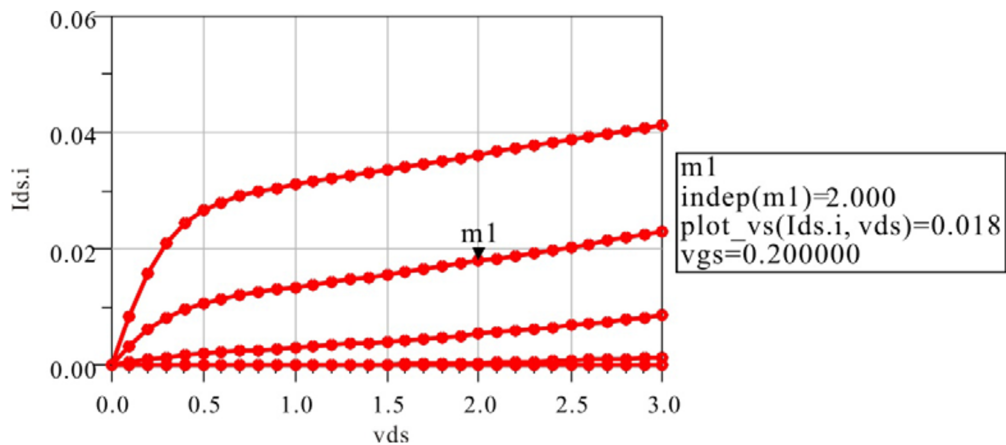


Figure 5E.6 DC characteristics of pHEMT FHX15

Setting the bias for I_{DS}=18 mA, S-parameter simulation is performed as shown in Fig. 5E.7. In order to obtain the simplified FET equivalent circuit values using the obtained S-parameters, the following equations shown in Fig. 5E.8 are entered in the Display window.

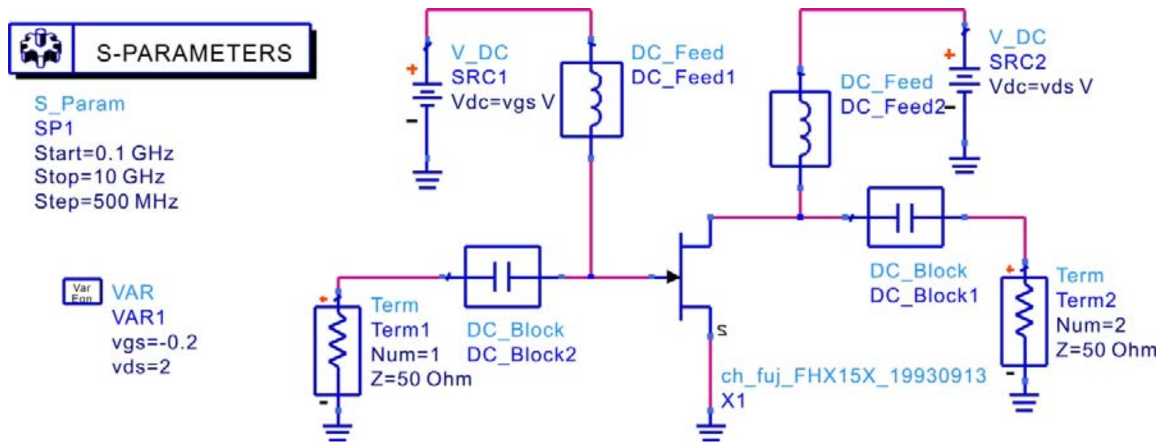


Figure 5E.7 S-parameter simulation circuit

```
Eqn w=2*pi*freq
Eqn Cgd=imag(-Y(1,2))/w
Eqn Rds=1/real(Y(2,2)+Y(1,2))
Eqn Cgs=-1/(w*(imag(1/Y(1,1)+Y(1,2))))
Eqn Cds=1/w*imag(Y(2,2)+Y(1,2))
Eqn Ri=real(1/Y(1,1)+Y(1,2)))
Eqn gm=-mag((Y(2,1)-Y(1,2))/(Y(1,1)+Y(1,2)))/imag(1/(Y(1,1)+Y(1,2)))
Eqn tau=(-1/w)*phase(j*(Y(2,1)-Y(1,2))/(Y(1,1)+Y(1,2)))
```

Figure 5E.8 Equations for obtaining the values of the simplified equivalent circuit

Using these equations and plotting for each equivalent circuit value with respect to frequency, the following results shown in Figs. 5E.9, 5E.10, and 5E.11 are obtained.

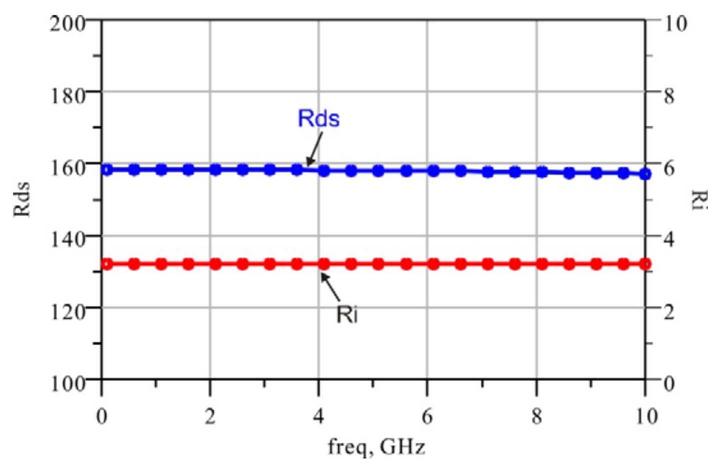


Figure 5E.9 Computed **Rds** and **Ri** results

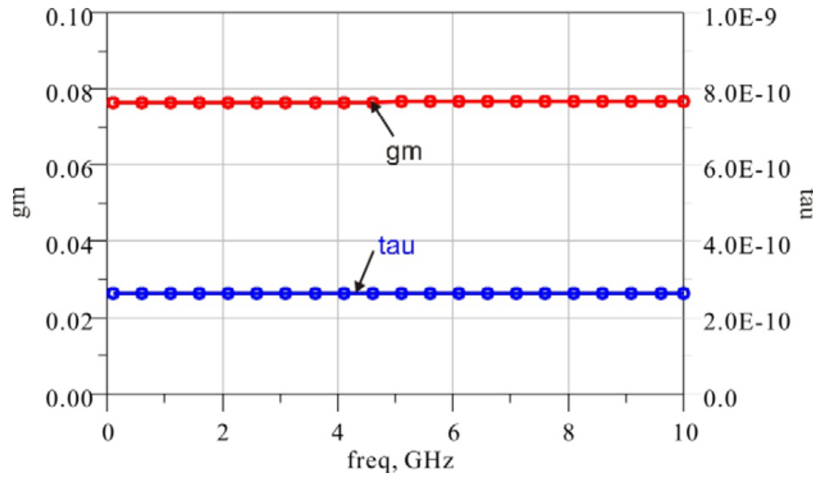


Figure 5E.10 Computed **gm** and **tau** results

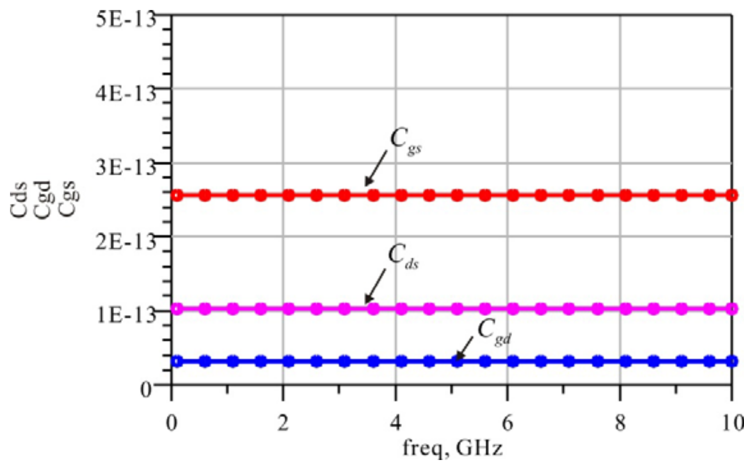


Figure 5E.11 Computed **Cgs**, **Cgd** and **Cds** results

From the results of Figs. 5E.9 to 5E.11, we see that, g_m=77mS, τ=0.26 ns, R_{ds}=158 ohm, C_{gs} =0.25 pF, C_{gd}=31 fF, and C_{ds}=0.1pF.

■

From Example 5.2, we can determine the simplified FET equivalent circuit. Figure 5.37 shows again the equivalent circuit of a chip FET. The equivalent circuit is known to quite closely predict the measured S-parameters of a chip FET. The difference between the chip FET and simplified equivalent circuits are in R_g, R_s, and R_d, which are called extrinsic elements. In order to determine the chip FET equivalent circuit, the method similar to the extraction of the simplified equivalent circuit does not exist at present. The values of R_g, R_s, and R_d were previously determined by optimization technique using the measured S-parameters. However, because these resistors in the active state of a FET make only little contribution to the S-parameters, the uncertainty of the values

thus determined is large, and it is difficult to determine the exact values. If we assume that R_g, R_s, and R_d does not change even when the operating point changes, their values may be determined more accurately using the measured S-parameters at the operating point at which the effect of these resistors are dominant. Thus, such operating point should be found first, from which the value of the resistors can be extracted more accurately.

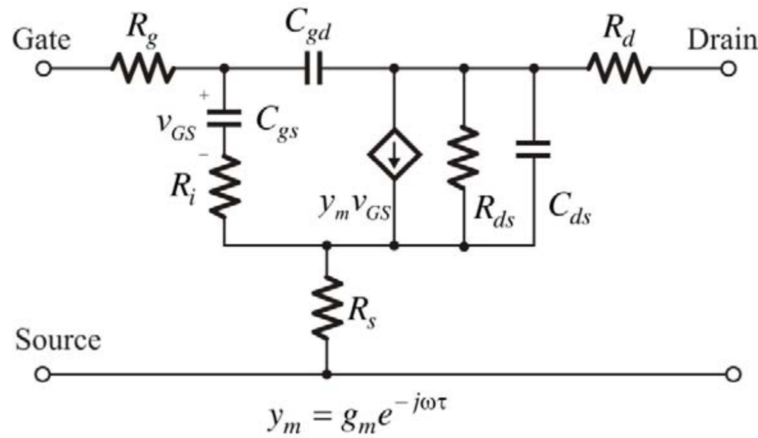


Figure 5.37 Small-signal equivalent circuit of chip FET

The operating point of V_{gs}=0 and V_{ds}=0 is thought to be suitable. At this bias point, the FET completely becomes a passive device, and the equivalent circuit appears as shown in Fig. 5.38. The zero bias depletion capacitance C_b appears, and will show the same value to the source and drain sides. Because there is no change in the values of R_g, R_s, and R_d, these values are the same as in active mode. This is often referred to as cold-FET measurement. [11]

Even in this condition, the values of R_g, R_s, and R_d are typically small, and because the impedance of the depletion capacitance C_b is usually very large, it is difficult to accurately determine these values when measurement errors occur.

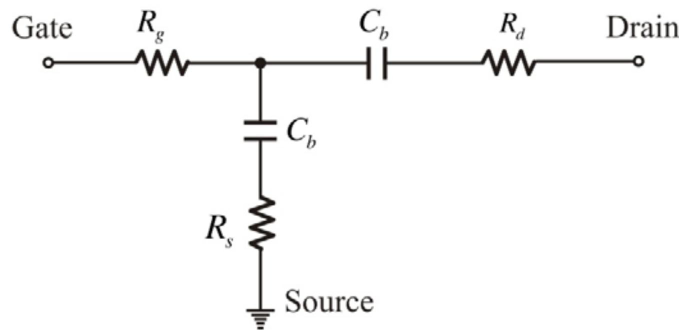


Figure 5.38 FET small-signal equivalent circuit for V_{gs}=0, V_{ds}=0

To overcome this problem, a small positive voltage is applied to the gate terminal, and this makes the gate-drain and gate-source behaves as Schottky diodes. These diodes begin to conduct and so the contribution of C_b disappears. Instead, a small-signal resistance of a Schottky diode is formed. In addition, the channel resistance is formed between the drain-source. Since the effect of

the channel resistance appears in a distributed form, it must be considered as a distributed circuit. However, their distributed effect is not pronounced and so they can be regarded as lumped elements. With channel resistor considered the Z-parameters are [11]

$$z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} \tag{5.40}$$

$$z_{12} = R_s + \frac{R_c}{2} \tag{5.41}$$

$$z_{22} = R_s + R_d + R_c \tag{5.42}$$

Resistor R_c represents the channel resistance, and nkT/qI_g of z_{11} represents the small signal Schottky diode resistance dependent on the DC gate current I_g. The different contributions of the channel resistances on z_{11}, z_{12}, and z_{22} are because the effect of the distributed channel resistance yields different contribution to z_{11}, z_{12}, and z_{22}. From equations (5.40) to (5.42), it can be found that z_{11} alone depends on the small signal Schottky diode resistance. Thus, the term excluding the small signal Schottky diode resistance can be found plotting Re(z_{11}) *vs*. the diode current I_g. Figure 5.39 shows a plot of Re(z_{11}) *vs*. the diode current I_g. Using the plot, the term excluding the small signal Schottky diode resistance is found from the intercept value obtained by extending the straight line.

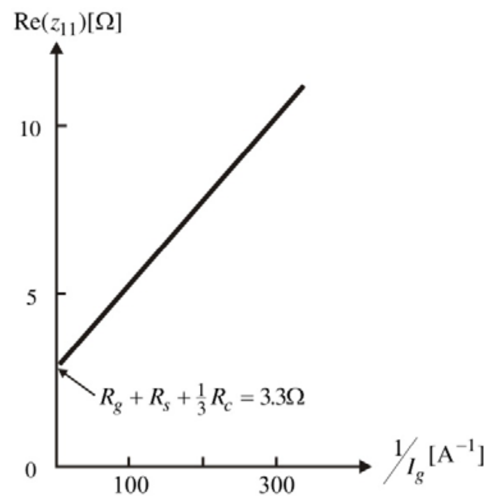


Figure 5.39 Plot for obtaining R_g+R_s+1/3·R_c (reference [11])

However, from the resulting equations, the desired values of R_g, R_s, and R_d cannot be determined because there are four unknowns but three equations. Therefore, a separate independent measurement is required. There are two methods. One way is using 1) the Fukui method, the value of R_s+R_d can be determined through this method. The other is to 2) directly measure the DC gate resistance in the device. After the values of R_g, R_s, and R_d are determined through such cold-FET measurement, the remaining values of the chip FET equivalent circuit in Fig. 5.37 can be obtained using the measured S-parameters in active mode. Figure 5.40 shows the method of extracting the

contribution of these resistors from the measured S-parameters in the active mode. Then, the remaining circuit is a simplified FET equivalent circuit (or intrinsic equivalent circuit of a FET). By converting the resulting S-parameters into Y-parameters, the values of the simplified equivalent circuit can be determined as shown in Example 5.2.

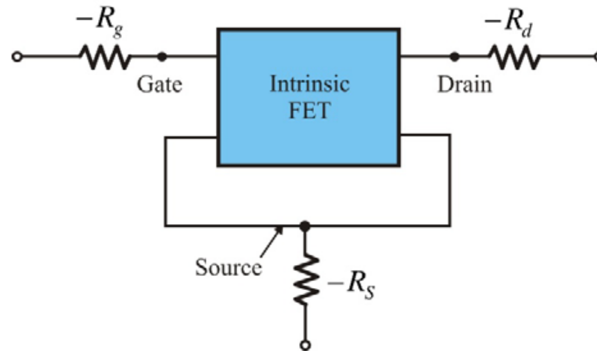


Figure 5.40 Method of removing the effect of resistors R_g, R_s, and R_d in the measured S-parameters

■ Example 5.3

In Example 5.2, the values of R_g, R_s, and R_d were approximated to 0 to extract the simplified FET equivalent circuit of the pHEMT FHX15 at V_{DS}=2V and V_{GS}=–0.2V. When R_g=1.4, R_s=1.5, and R_d=1.5 ohm, determine the values of the simplified FET equivalent circuit with the effect of these resistors removed.

Solution

Figure 5E.12 shows a circuit setup to remove the effect of the resistances R_g, R_s, and R_d. The Data Component is the calculated S-parameters in the aforementioned Example 5.2. In addition, the calculation of Y-parameters in the S-parameter simulation controller is checked.

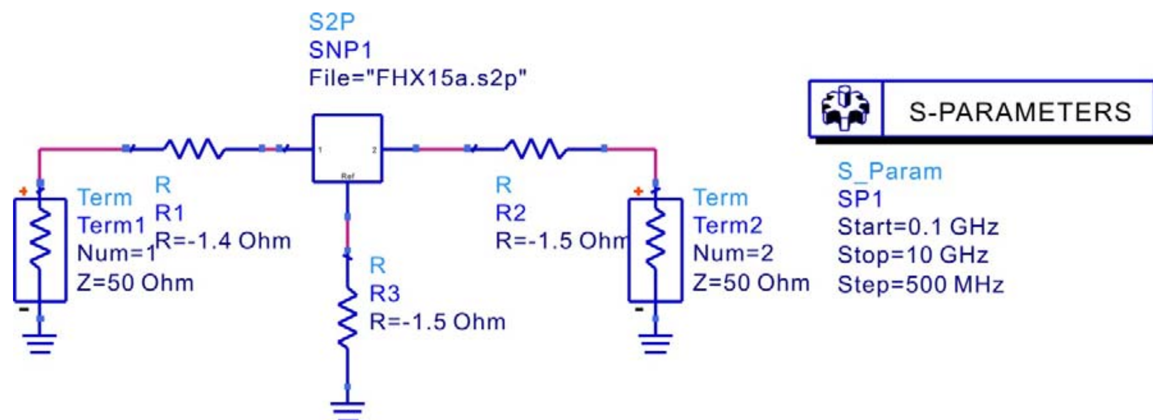


Figure 5E.12 Circuit for removing the effect of the resistances R_g, R_s, and R_d

In addition, the formulas in Fig. 5E.8 are entered again in the Display window. In that case, the changed values of the simplified FET equivalent circuit can be recalculated. The computed values

of the equivalent circuit are g_m=88 mS, τ=0.25 ns, R_{ds}=137 ohm, C_{gs}=0.28 pF, C_{gd}=29 fF, and C_{ds}=0.12 pF. The general trend is that the resistance values are reduced while the capacitor values increase. The frequency dependences of the computed results are not appreciable, the values simply move up and down. The change in trans-conductance value is especially noteworthy as it is directly related to the gain. It can be seen that, the change Δg_m=11 mS. This comparison is shown in Fig. 5E.13.

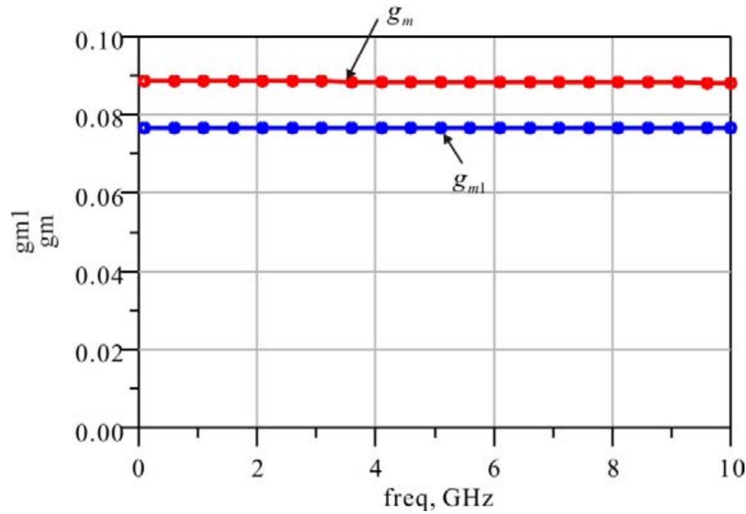


Figure 5E.13 Changes in **gm** due to the effects of R_g, R_s, and R_d.

In Fig. 5E.13, g_m represents the current compensated result for R_g, R_s, and R_d while g_{m1} is the result obtained in the previous example, which does not consider the effects of the parasitic resistors. Here, it is generally known that R_s is the main reason for this reduction in g_m; g_m is reduced by R_s as shown below:

$$g_m = \frac{g_m^o}{1+g_m^o R_s} = \frac{88}{1+0.088\times 1.5} = 77 \text{ mS}$$

We can see that this is the same as calculated in Example 5.2. Therefore, in order to prevent the reduction of g_m by R_s in a large trans-conductance FET, special attention must be taken to make R_s smaller.

■

REFERENCES

[1] G. D Vendelin, A. M. Pavio, and U. L. Rohode, *Microwave Circuit Design using linear and nonlinear techniques*, John Wiley& Sons Inc., 1990.

[2] G. Gonzalez, *Microwave transistor amplifiers analysis and design*, 2nd edition, Prentice Hall, 1997.

[3] R. Soares, J. Graffeuil, and J. Obregon, *Applications of GaAs MESFETs*, Artech House Inc., 1983.

[4] J. M. Golio, *Microwave MESFETs and HEMTs*, Artech House, 1991.

[5] J. Mun ed., *GaAs Integrated Circuits*, BSP Professional Books, 1988.

[6] H. Fukui ed., *Low noise Microwave Transistor & Amplifiers*, IEEE Press, 1981.

[7] G. Massobrio and P. Antognetti, *Semiconductor Device modeling with SPICE*, 2nd ed., McGraw Hill, 1993.

[8] Marcuvitz, *Waveguide Handbook*

[9] K. W. Yeom, T. S. Ha, and J. W. Ra, "Frequency dependence of GaAs FET Equivalent circuit Elements extracted from the measured two port S-parameters," *Proc. IEEE*, vol. 76, no. 7, pp. 843-845, July 1988.

[10] R. L. Vaitkus, "Uncertainty in the values of GaAs MESFET equivalent circuit elements extracted from the measured two-port scatttering parameters," *1983IEEE Cornell Conference on High Speed Semiconductor Devices and Circuits*, Cornell Un., August, 1983.

[11] G. Dambrine, A. Cappy, F. Helidore, and E. Playez, "A new method for determining the FET small signal equivalent circuit," *IEEE Trans on Microwave Theory and Tech*., vol. 36, no. 7, pp. 1151-1159, July 1988.

[12] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," *Bell Syst. Tech. J*., vol. 58, no. 3, pp. 771-795, 1979.

PROBLEMS

5.1 Figure 5P.1 shows a simplified equivalent circuit of GaAs MESFET at low frequency.

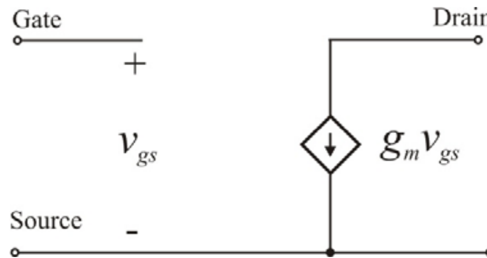


Figure 5P.1 A simplified FET equivalent circuit

(1) Calculate S-parameters setting the reference impedance Z_o.
(2) Setting Z_o =50 ohms, compute g_m when $S_{21}=5\angle 180°$.
(3) When resistor R_f is connected in parallel as shown in Fig. 5P.2, find the value of R_f that makes $S_{11}=0$.

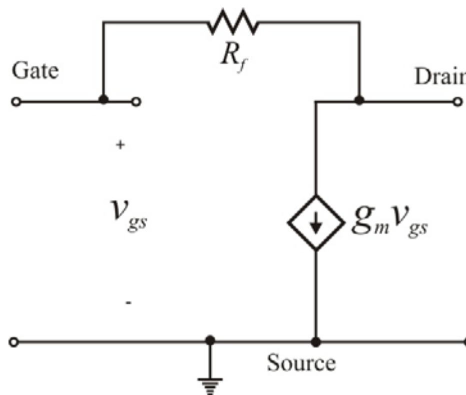


Figure 5P.2 A simplified FET equivalent circuit with a parallel feedback resistor

5.2 Figure 5P.3 shows a simplified equivalent circuit of FET with source resistance R_s at low frequency. Due to R_s, the equivalent trans-conductance g_{me} is lowered from g_m as explained in Example 5.3. Defining the equivalent trans-conductance g_{me} as

$$g_{me} = \left.\frac{i_d}{v_{gs}}\right|_{\text{Drain shorted}}$$

Show that

$$g_{me} = \frac{g_m}{1 + g_m R_S}$$

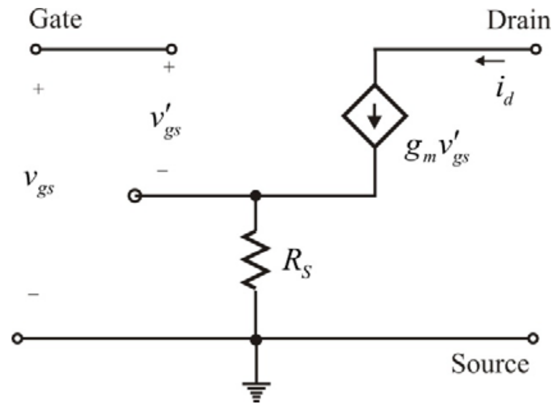
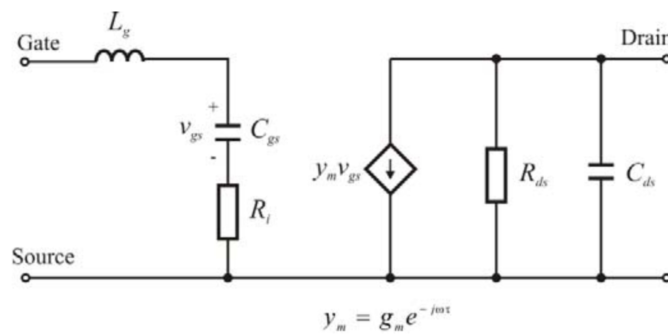
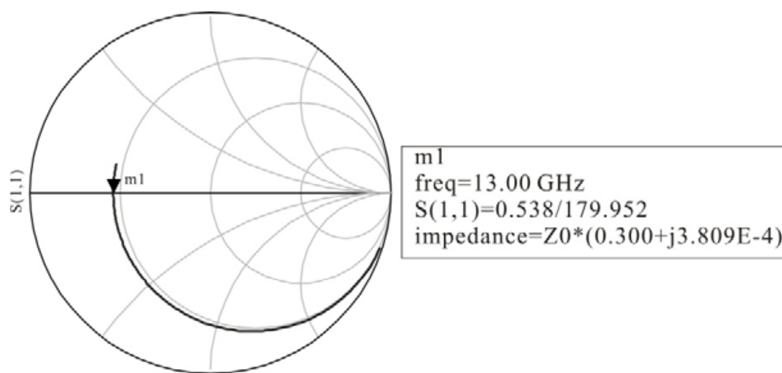


Figure 5P.3 A FET equivalent with a source resistor

5.3 The small-signal equivalent circuit of GaAs MESFET, including wire bonding, can be approximately represented by the figure below; given the following S_{11}, determine the values of R_i and L_g. (C_{gs}=0.5 pF)



(a)



(b)

Figure 5P.4 (a) GaAs FET equivalent circuit and (b) S_{11}

5.4 In the following active bias circuit, determine the value of resistor R_1 for a 20 mA current to flow into the transistor.

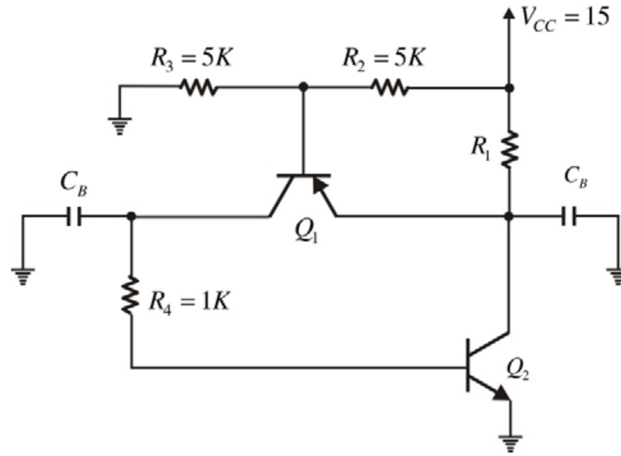


Figure 5P.5 Active DC bias circuit

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